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A 16 Channel Medium Speed Multiplexer

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1. INTRODUCTION

A medium speed multiplexer system that interfaces 16 synchronous serial channels to a Honeywell 16-bit series computer is described in this report. The system permits simultaneous communication between the Control Data 6600 computer, at the Courant Institute of Mathematical Sciences, and any 16 sites accessible by telephone or private line.

The salient features of the system are:

a. The multiplexer channels function with any synchronous data device in a half or full duplex mode.

b. The multiplexer channels handle data rates up to 10k bps.

c. The multiplexer channels are individually synchronized by the data channel clocks.

d. Eight-bit byte registration for a channel in the input mode is accomplished within the multiplexer. This feature can be bypassed for any channel if complete data transparency is desired.

e. Software overhead is less for 16 channel communication with the multiplexer/computer composite than with the computer alone and attendant interfaces.

f. The operating modes of each channel are controlled by the Honeywell computer software.

g. The data passing through the multiplexer, whether transmitting or receiving on any channel, is in no way altered. The philosophy of data transparency, a necessity in a research environment, is thus adhered to.

The multiplexer handles all remote batch entry of the CDC-6600. Figure 1 shows the CDC-6600/DDP-516 configuration* at the Computing Center.

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*The CDC-6600/DDP-516 interface and the remote entry system for the CDC-6600 are described in the following AEC Research and Development Reports published by New York University: Bianchini, R. P., "An Interface Between a Control Data 6600 Series Computer and a Honeywell 16-Bit Series Computer", NYO-1480-119, October 1969; Francheschini, E., Feinroth, Y., and Goldstein, M., "A Remote Entry System for the CDC-6600", NYO-1480-148, April 1970.

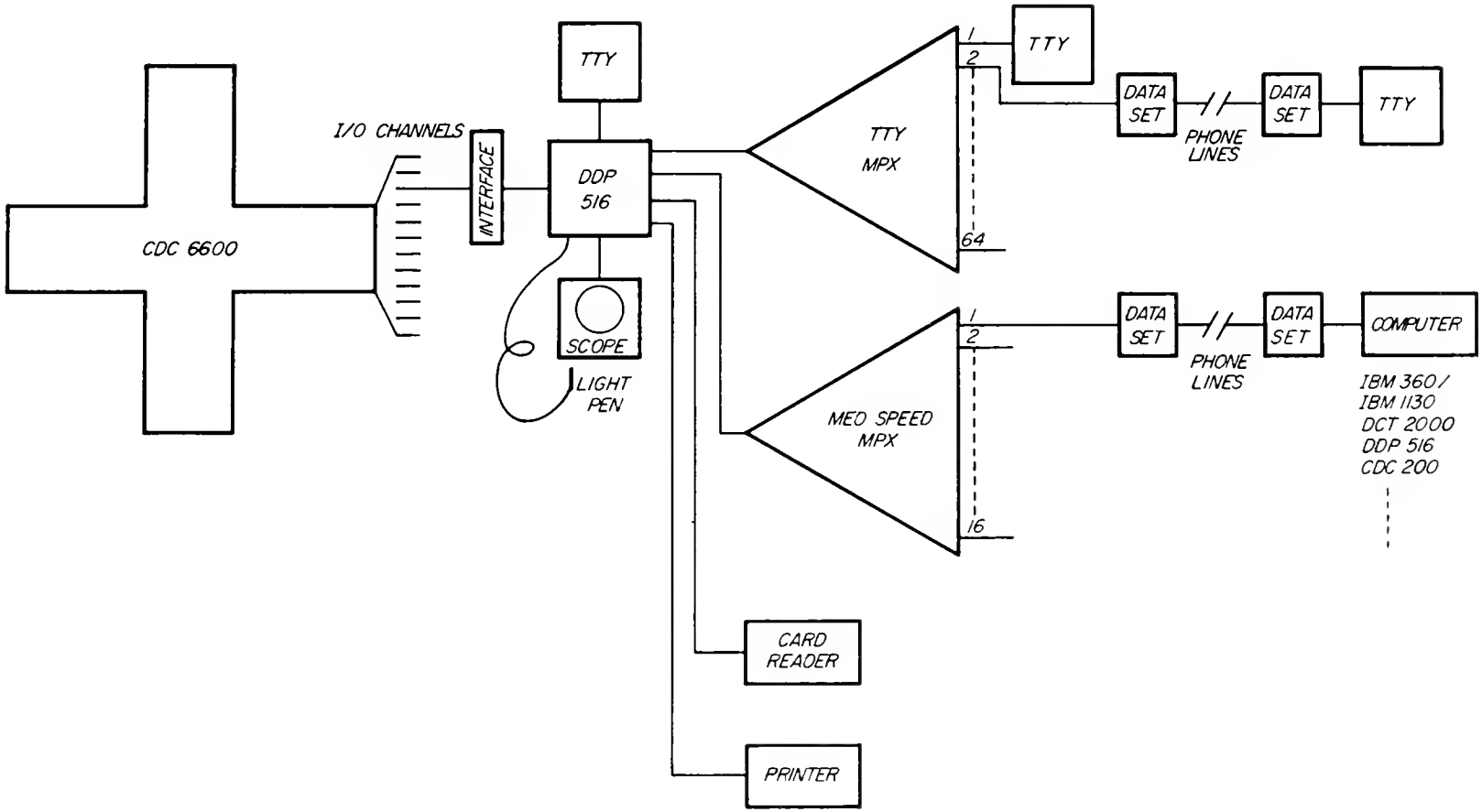


FIGURE 1 - 6600/516 CONFIGURATION

2. SYSTEM OPERATION

The remote entry configuration of the CDC-6600 consists of 16 synchronous serial channels interfaced by the multiplexer to a Honeywell 16-bit computer. The Honeywell computer is interfaced to the CDC-6600. This small "front end" computer, which is interfaced to the CDC-6600, performs the dual function of I/O controller and temporary storage. Any of the Honeywell models DDP-116/416/516 or H-316 can be used for this purpose.

The data to and from the serial channels is in the form of bit streams driven by channel clocks. The I/O structure of the Honeywell computer permits communication on a byte level. Therefore, the throughput of the multiplexer requires that it contain a memory. Since the multiplexer/computer communication is asynchronous, the multiplexer must be capable of communicating to the computer the real time requirements of the 16 serial channels. Accordingly, the multiplexer utilizes the hardware interrupt feature of the computer.

From an overall system point of view, the computer outputs data through the multiplexer to any one of the 16 serial channels. Transmission from computer to multiplexer is in 8-bit bytes. The multiplexer distributes the bytes as specified by the computer. Then the 8-bit bytes are marched out serially onto the appropriate channels. Since the channels are synchronized to channel trans-

mission clocks, the computer must maintain an output data rate of one 8-bit byte for every 8 counts of the corresponding channel transmission clock.

The computer collects data from any one of the 16 serial channels. The bit streams are synchronized to channel derived receive clocks. The multiplexer collects and stores the bits into groups of 8-bit bytes. The computer takes these bytes along with additional information for channel identification. Since the channels are synchronized to channel derived receive clocks, the computer must maintain an input data rate of one 8-bit byte for every 8 counts of the corresponding channel clock. While the bits are collected, the multiplexer hardware establishes the byte synchronization of the received message. The computer software is thus relieved of this task. A hardware switch can bypass this feature for any channel.

The multiplexer allows each of the 16 channels to operate independently. Thus, each channel may operate in a receive or transmit mode, at different data rates, in full or half-duplex, and with or without byte synchronization for received messages.

The computer interrupt circuitry controls the byte level communication between the computer and multiplexer. When the computer is interrupted for input, it collects the 8-bit bytes that the receive channels have ready. When the computer is interrupted for output, it outputs the 8-bit bytes that the multiplexer can accept for the channels in the transmit mode.

The multiplexer memory contains 48 bits for each channel: 24 for input and 24 for output data. In each case, double level byte buffering is employed. The design allows the computer an 8 bit time interval for servicing the multiplexer for input or output data. A real time hardware clock in the multiplexer paces the computer input and output interrupts. The real time bit requirements of the 16 serial channels determine the pacing rate.

Previous techniques would have required the computer to treat the 16 serial channels with individual 8-bit byte interfaces as separate devices, all with separate interrupts. This creates a software environment with a high interrupt overhead. The multiplexer has only two interrupts for all of the 16 serial channels: one for input, one for output. This feature reduces the interrupt software overhead that is required for communication between the 16 serial channels and the computer.

3. HARDWARE STRUCTURE

The multiplexer comprises four sections--see Fig. 2.

A. Clock, Timing, and Decode Circuitry. Synchronizes the delay line memory to the pre-multiplexer scanning and to the computer/multiplexer interface.

B. Pre-Multiplexer. Synchronizes each serial data channel to the multiplexer memory. Contains the individual channel mode selection switches.

C. Delay Line Memory. Consists of twelve 1 MHz delay lines for double level buffering of each of 16 channels. Each delay line has a 64 bit capacity.

D. Computer/Multiplexer Interface. Functions as a communication channel between the delay line memory and the computer. Can buffer an 8-bit byte for computer input and output data. Buffering is necessary because of the 64 μsec access time of the delay line memory.

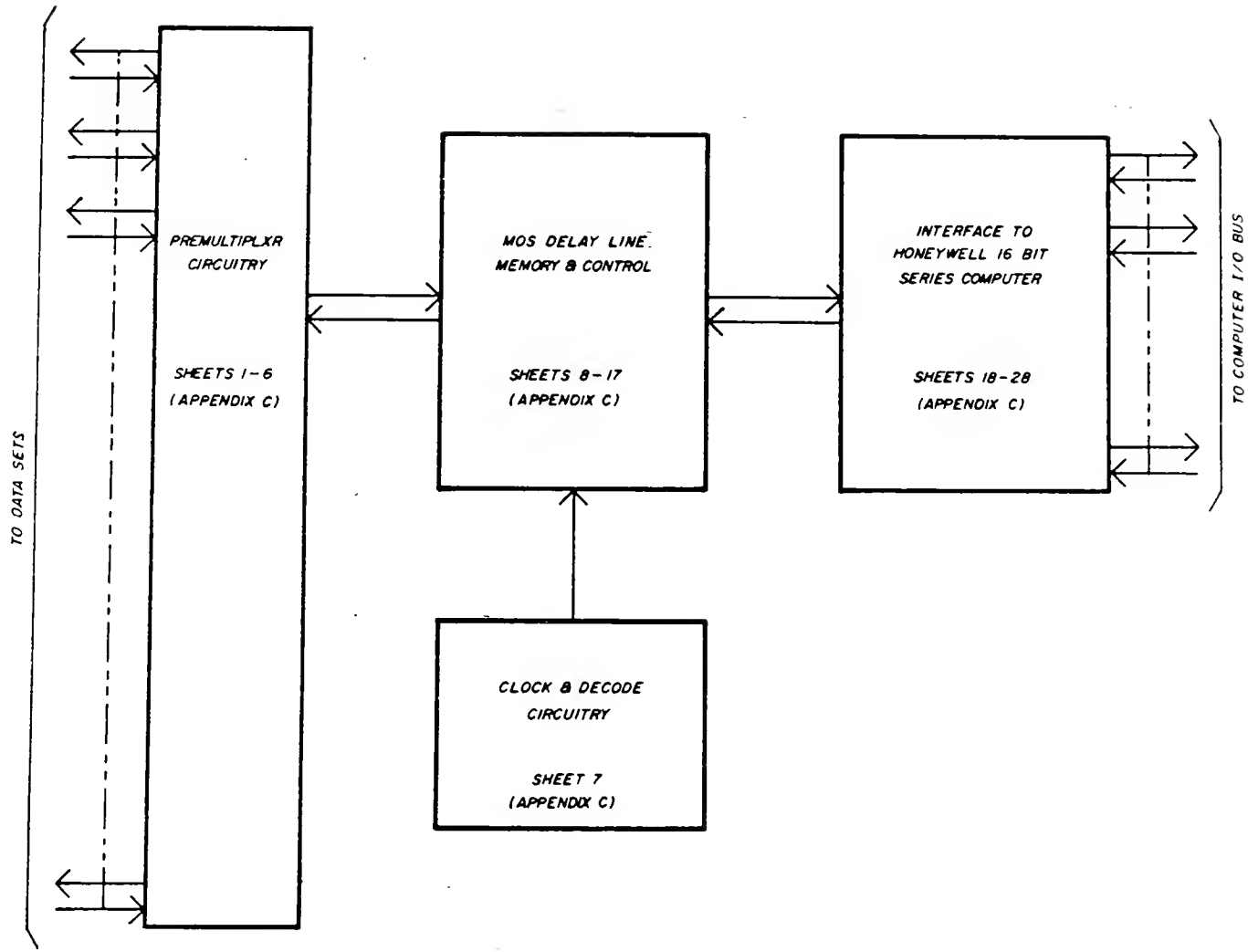


FIGURE 2 - SYSTEM BLOCK DIAGRAM OF 16 CHANNEL MULTIPLEXER

3A. Clock, Timing, and Decode Circuitry

(See Appendix C Schematics, Sheet no. 7)

Contains a 1 MHz crystal control clock, a 6 bit countdown chain, a 2 bit decoder, and a 4 bit decoder. The 2 bit decoder cycles every 4 clock counts; the 4 bit decoder cycles every 64 clock counts. See Fig. 3. Since the 1 MHz clock drives the delay lines, one cycle of the 4 bit decoder corresponds to one delay line trip. Fig. 4 shows the timing relationship of all the clock outputs. The 4 bit decoder has sixteen 4 μsec states: 00_8, 01_8, 02_8, 03_8,...17_8. Each state has four 1 μsec sub-states: T0, T1, T2, and T3. Thus in the sequential time allocation of the 16 data set channels, the time slice for each is subdivided into four 1 μsec sub-states: T0, T1, T2, and T3.

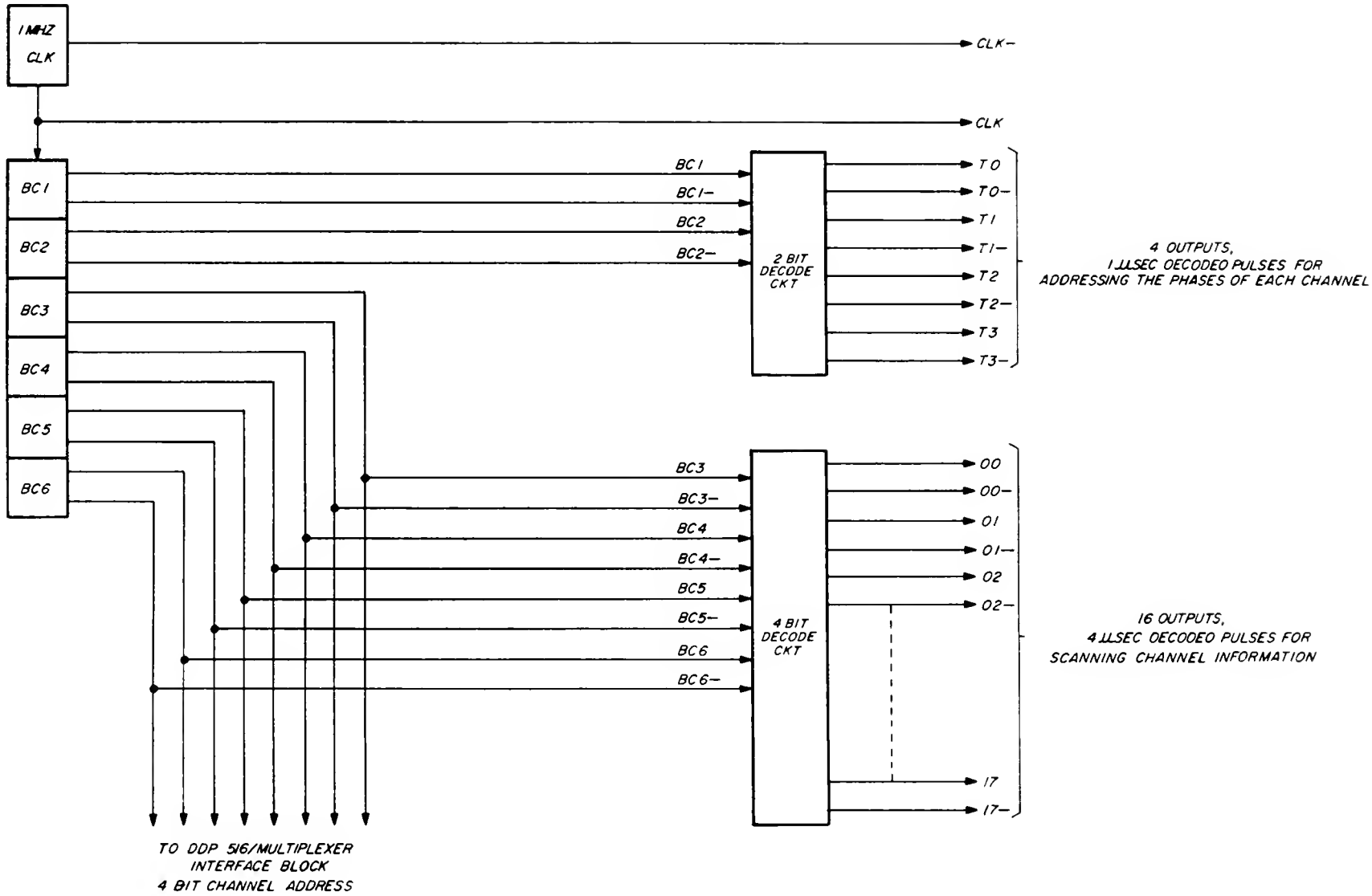


FIGURE 3 – SYSTEM CLOCK AND DECODE CIRCUITRY

TIMING WAVESHAPES GENERATED BY CLK, DEC CIRCUITRY

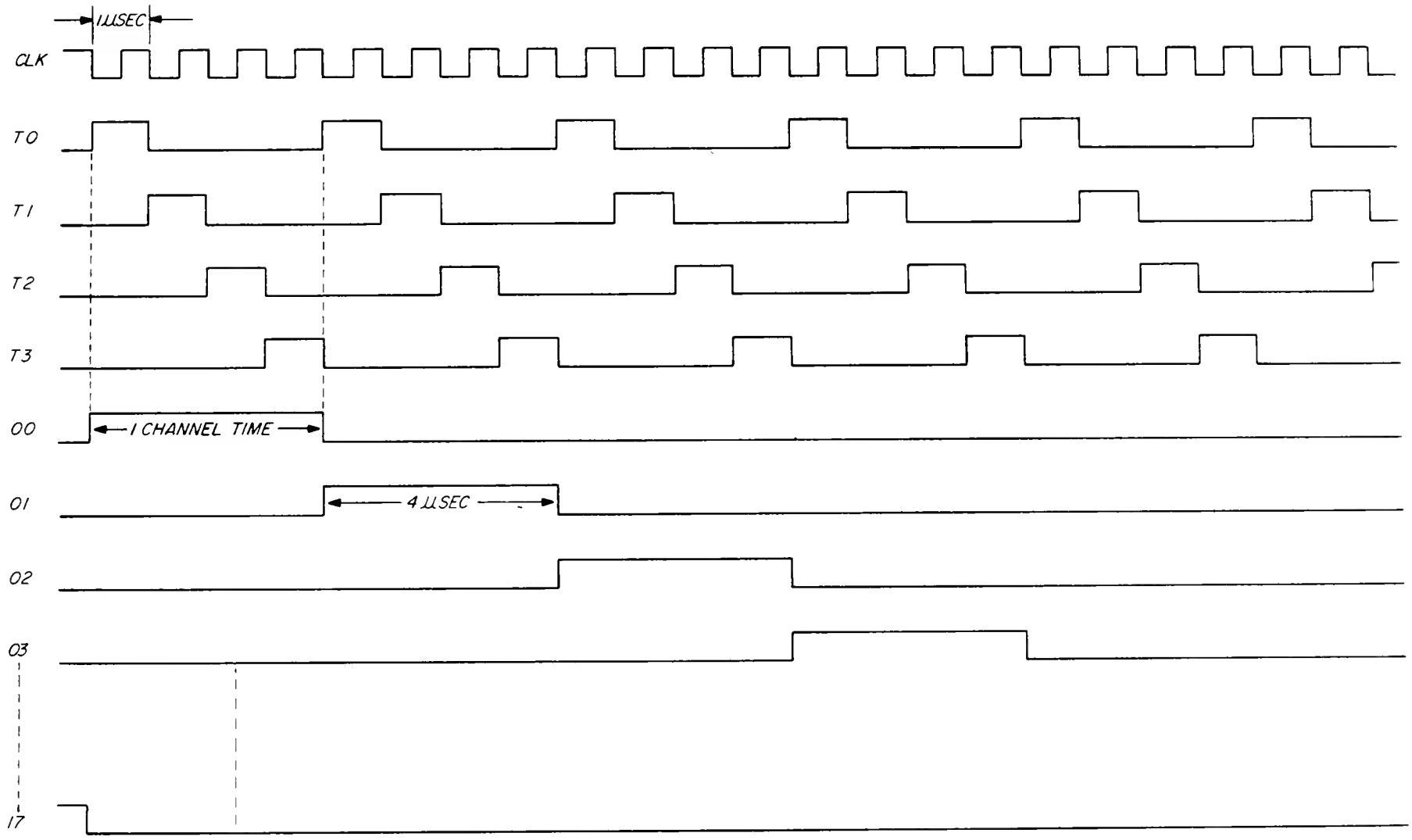


FIGURE 4

3B. Pre-Multiplexer Circuitry

(Appendix C Schematics, Sheets 1-6)

Each pre-multiplexer channel comprises seven flip-flops, "nand" gates for scanning and control, and level convertor circuits for voltage compatability between the pre-multiplexer and the synchronous serial data channels.

Two flip-flops are used for channel mode selection, and are separately controlled by the computer software. Two flip-flops are used for receiving serial data from the channel. Three flip-flops are used for transmitting serial data onto the channel.

Data Terminal Ready Flip-Flop

In the "1" state, enables the channel to operate. In the "0" state, closes off the logic and disconnects the channel from the remote user.

Request to Send Flip-Flop

In the "1" state, sets the channel into the transmit mode. In the "0" state, sets the channel into the receive mode. The state of this flip-flop is forced by a hardware switch when the channel is used in a full-duplex mode.

Receive Data and Receive Clock Flip-Flops

The receive data flip-flop functions as a one-bit serial buffer. The receive clock flip-flop functions as a switch which is set by the channel receive clock. The switch remains set until the delay line memory can accept the bit from the receive data flip-flop. This can occur only during the 4 μsec time slice assigned to the channel.

Transmit Clock and Two Transmit Data Flip-Flops

The transmit clock flip-flop functions as a switch which is set by the channel transmit clock. The switch remains set until the delay line memory can output data to the two transmit data flip-flops. The two flip-flops function as a two bit serial buffer which outputs data to the channel at a rate determined by the transmit clock.

3C. Delay Line Memory

(Appendix C Schematics, Sheets 8-17)

This section of the hardware contains the memory required for control and double level buffering of all of the 16 serial data channels. The receive buffers are used with a compare circuit to establish byte synchronization of the receive message. The memory consists of 64 sequential 12-bit words. A new word is accessed from the sequential memory at a 1-μsec rate. The total cycling time of the memory is 64 μseconds. Four of the 12-bit words are used for handling data bits of each serial data channel.

Channel bit storage requirements are shown in Tables I and II, p. 17-19. Delay line memory bit assignments are shown in Fig. 5. The first two words, T0 and T1, are used for channel receive data. The second two words, T2 and T3, are used for channel transmit data. Because of the sequential nature of the memory, byte transfers from T0 to T1 and T2 to T3 are accomplished by using an 8-bit data delay register (8 flip-flops). Accordingly, in the receive mode, the channel data collection buffer T0 precedes the byte static buffer T1; in the transmit mode, the channel data distribution buffer T3 follows the static buffer T2.

The combination of serial and parallel 8-bit buffers, for input and output, forms the double level buffering mechanism for each channel. The byte static buffers store 8-bit bytes. The serial

buffers satisfy the real time requirements of the serial data channels (one bit per channel clock interval).

The delay line memory consists of the following circuitry plus interconnecting logic and flip-flops--see Fig. 6.

8-Bit Data Register

This register is inserted between the output and input of the delay line memory. It is used to transfer byte data from the serial buffer to the byte static buffer (receive mode), or from the byte static buffer to the serial buffer (transmit mode). These transfers take place when the input serial buffer goes full, or when the output serial buffer goes empty.

Synch Compare Circuitry

Establishes the first bit of a receive message. The circuit compares the contents of the receive serial buffer against a known pattern (synch), as the receive bit stream is marching through the receive serial buffer.

Add "1" Logic

Six bits for each channel are reserved in memory to store two separate 3 bit counts. One set is for the number of receive serial buffer shifts, the other is for the number of transmit serial buffer shifts. The add "1" logic updates these counters every time data is shifted.

Twelve 64-Bit Delay Lines

Each delay line is a 64-bit MOS 1 MHz shift register. A stored bit can only be read when it is shifted out of the end of the delay line. By feeding the delay line output back into the input logic gates, a bit can either be stored indefinitely or modified as required. An expandable "or" node is provided at the input of each delay line. This allows for the addition of as many control functions as needed. The 12 delay lines operate in parallel; therefore, at any one time, a 12-bit word is read out by looking at the output of each of the delay lines. Because of the output to input feedback, this word can be either stored indefinitely or modified. When clocking these lines at a 1 MHz rate, a new 12-bit word appears at the outputs of the delay lines every one μsecond. Since these lines are 64 bits long, a particular 12-bit word is accessible every 64 μseconds. At this point, it can either be modified or reinserted as is into the lines. The lines operate in complete synchronism with the scanning of the 16 pre-multiplexer channels. Each pre-multiplexer is allowed a 4 μsec time slice--Fig. 7. During this time slice 4 sequential, 1 μsec 12-bit words of delay line memory are accessible. This occurs for each pre-multiplexer channel every 64 μseconds.

Table I - Input Data Bits For Each Serial Channel

1. 7 bits are used as a serially loaded, parallel-out shift register buffer. The buffer shifts in data at a rate equal to the receive channel clock.

2. 8 bits are used as a parallel-in, parallel-out byte static buffer.

3. 3 bits are used to store the number of shifts of the receive serially loaded buffer. The count is updated by 1 for each shift of the serial buffer.

4. Full bit. This is a switch which is set when the serial buffer is full, and its contents are transferred to the static buffer. This occurs when the 3-bit stored count cycles through its zero state. The switch is reset when the multiplexer/computer interface can accept the 8-bit byte from the byte static buffer.

5. 2 bits are used to establish the first bit of the receive message. These are the pre-synch and synch bits.

6. 2 bits are used to mark the first bit of the receive message, and to send a termination word to the computer when the serial

channel is no longer receiving data. These are the start and stop bits.

7. Overwrite bit. This is a switch which is set when the computer fails to meet the receive real time byte requirements of the serial channel.

Table II - Output Data Bits For Each Serial Channel

1. 8 bits are used as a parallel-in, parallel-out byte buffer.

2. 8 bits are used as a parallel-in, serial output shift register. This buffer shifts out data at a rate equal to the transmit channel clock.

3. 3 bits are used to store the number of shifts of the transmit serial output buffer. The count is updated by 1 for each shift.

4. Empty bit. This is a switch which is set when the serial output buffer is empty. At this point, an 8-bit byte is transferred to it from the byte static buffer. This occurs when the 3-bit stored count cycles through its zero state. The switch is reset when the multiplexer/computer interface loads the static buffer with another 8-bit byte.

5. Underwrite bit. This is a switch which is set when the computer fails to meet the transmit real time byte requirement of the serial channel.

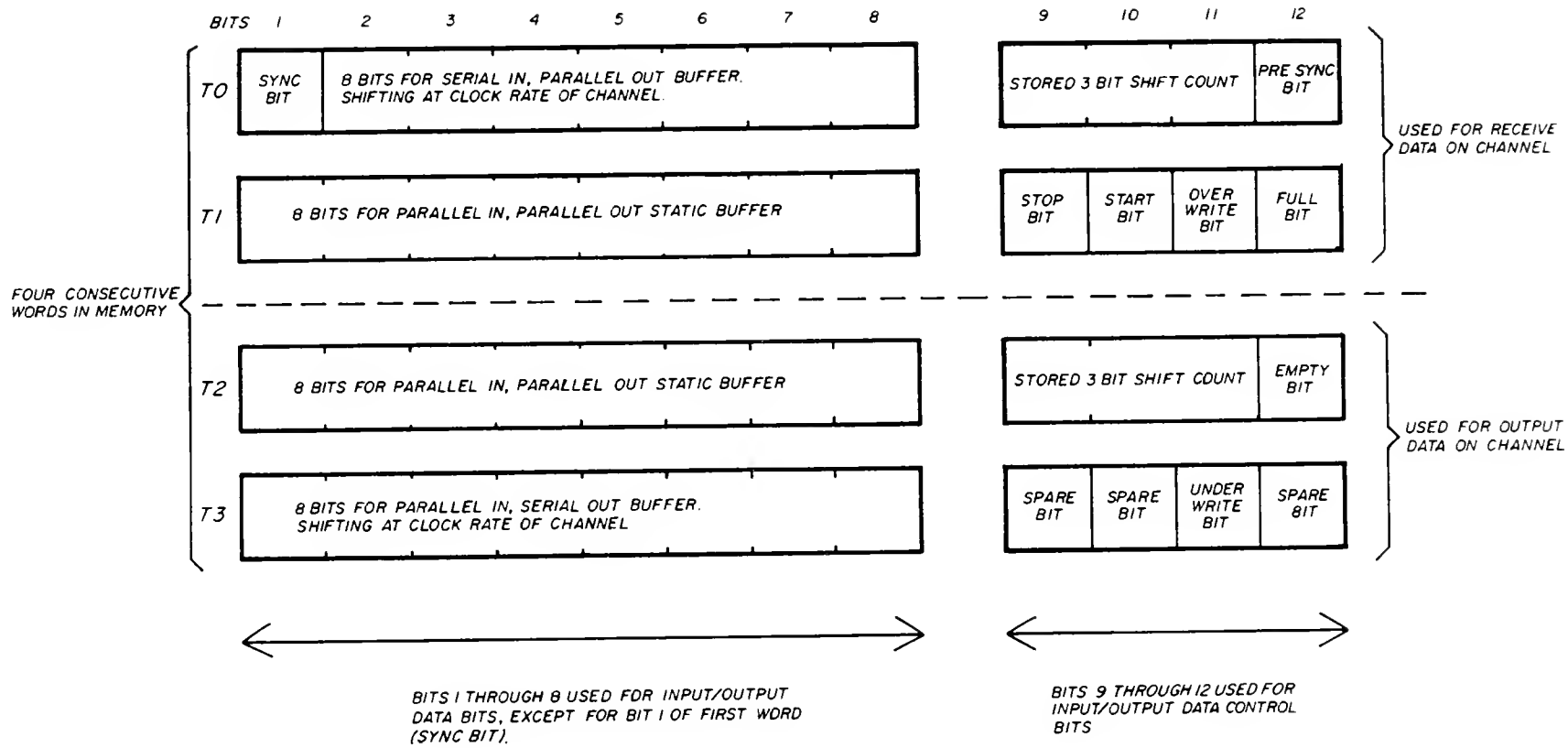


FIGURE 5 - BIT ASSIGNMENTS IN MEMORY FOR HANDLING ONE OF SIXTEEN SERIAL CHANNELS. TOTAL MEMORY REQUIREMENT IS 64 TWELVE BIT WORDS.

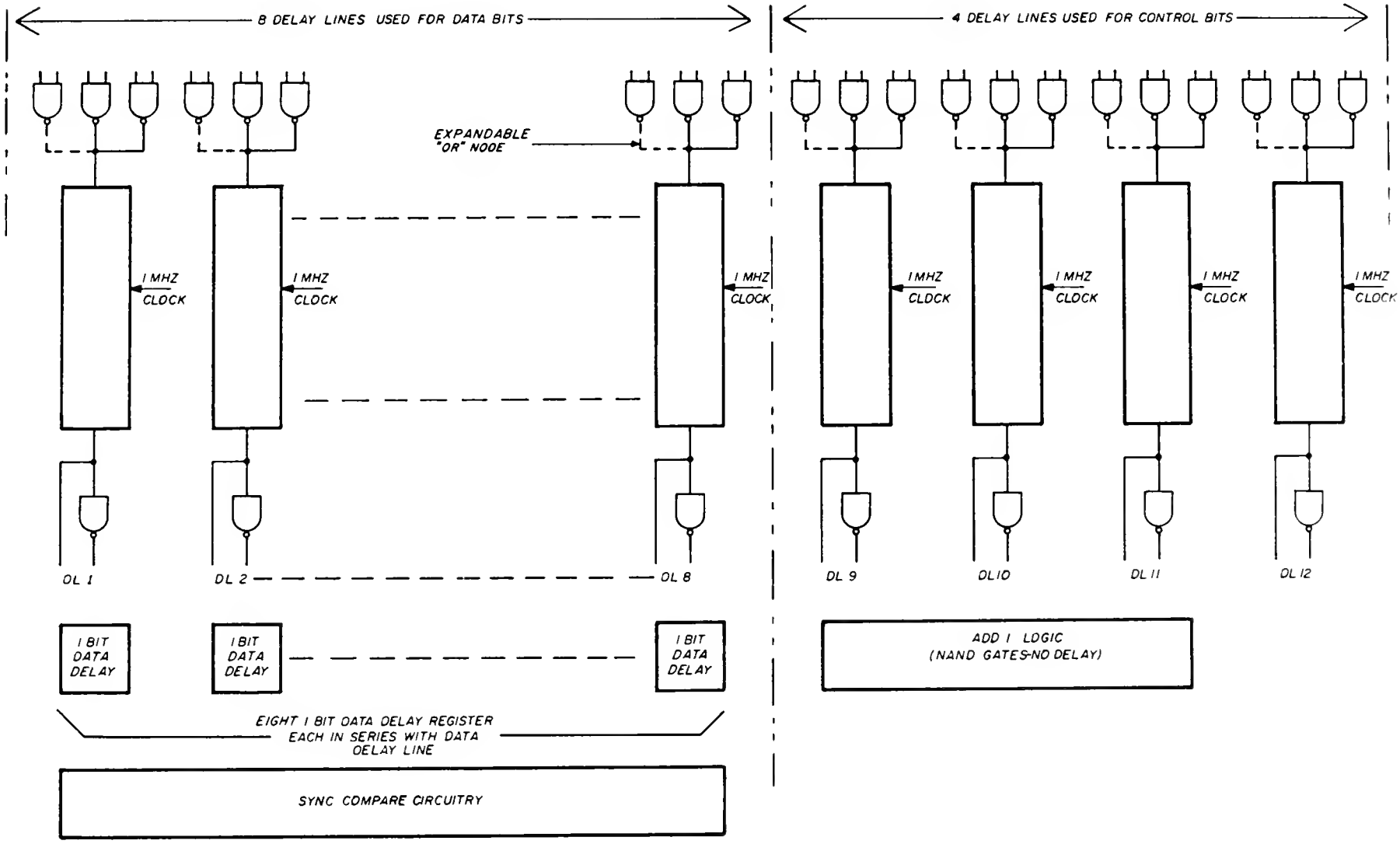
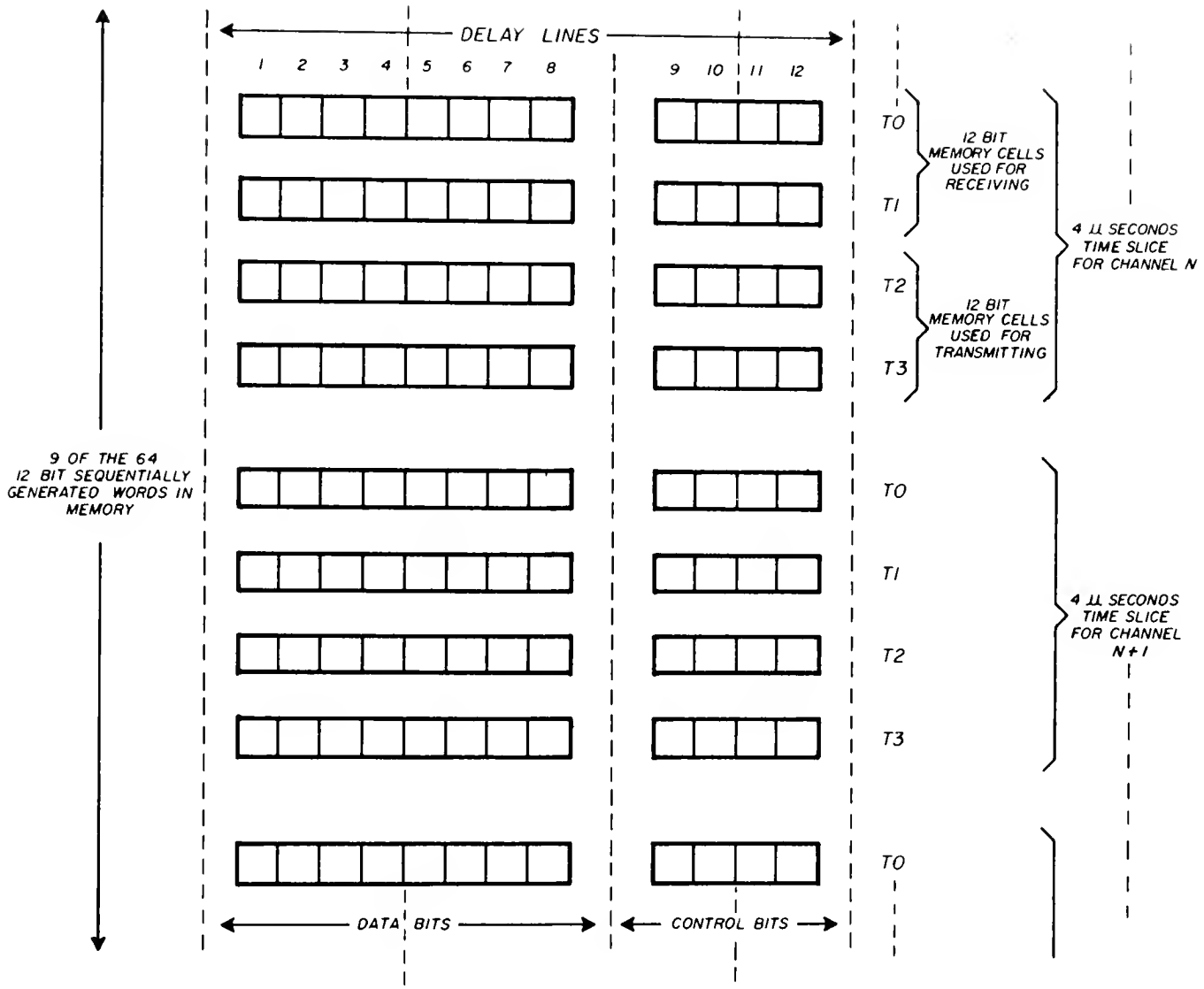


FIGURE 6 – DELAY LINE MEMORY



MEMORY SYSTEM IS SYNCHRONIZED TO THE PRE-MULTIPLEXER CHANNEL SCANNING SYSTEM. THEREFORE A GIVEN PRE-MULTIPLEXER CHANNEL HAS ACCESS TO ONLY ONE GROUP OF FOUR 1μSEC WORDS (TO,TI,T2,T3). 16 CHANNELS ARE HANDLED BY THIS SEQUENTIALLY CONSTRUCTED MEMORY.

FIGURE 7 - MEMORY SYNCHRONIZATION

3D. Computer/Multiplexer Interface
(Appendix C Schematics, Sheets 18-28)

This section of the hardware contains two interfaces. They interface the delay line memory receive and transmit byte static buffers to the I/O bus of the computer. One interface contains the input data register, and the other the output data register. These registers provide the computer I/O bus with access to the delay line memory. A real time clock is used to pace the computer hardware interrupts for the 2 registers. The frequency of the clock depends upon the real time requirements of the channel with the highest bit rate.

Input Data Register System (Appendix C Schematics, Sheets 18, 19, 23)

When the byte storage buffers (word T1, Fig. 7) of the delay line memory become full, they compete for the input data register. When one byte is in this register, bytes are gated out until the register goes empty. The full condition of this register is gated with the pacing circuit. This generates an interrupt that causes the computer to enter an input routine.

When the input data register goes empty, it is ready to accept new bytes from the delay line memory. The process of the delay line memory emptying its byte storage buffers into the input data register continues until all receive byte buffers are empty.

As byte data is transferred from the delay line memory to the input data register, 4 bits from the clock, timing, and decode circuitry are strobed into 4 flip-flops of the register for channel identification. An additional 4 bits are strobed in the register. These are the overwrite, underwrite, start, and stop bits--see Fig. 5.

The overwrite and underwrite bits are set only when the computer fails to satisfy the real time byte requirements of the channel for either the receive or transmit mode. The start bit is set to indicate to the computer the first byte of the receive message. The stop bit is set when the channel stops receiving.

Output Data Register (Appendix C Schematics, Sheets 20, 25-27)

When the byte static buffers (word T2, Fig. 7) of the delay line memory go empty, an empty-flag is set in the 16-bit delay line status register--Fig. 9. The empty-flag corresponds to the channel that went empty. The flag "or" output is gated with the pacing circuit for computer interrupt operation. The computer senses this empty-flag, and the empty/full status of the output data register--Fig. 9. When the register is empty and the empty-flag is set, the computer is allowed to output a word for the corresponding transmitting channel. The computer output word is in the format shown in Fig. 9. The successful execution of this output resets the empty-flag in the 16-bit delay line status register. The empty-flag that gets reset is determined by the transmit channel 4-bit address, as indicated in the word format.

With the 16-bit delay line status register, the computer does not have to access the delay line memory (64 μsec access time) to check the empty/full status of a given byte static buffer. The register allows the computer to sense the condition without any memory (delay lines) access time. The importance of knowing this condition in advance is to prevent the computer from placing data, which the delay line memory will not accept, in the output data register.

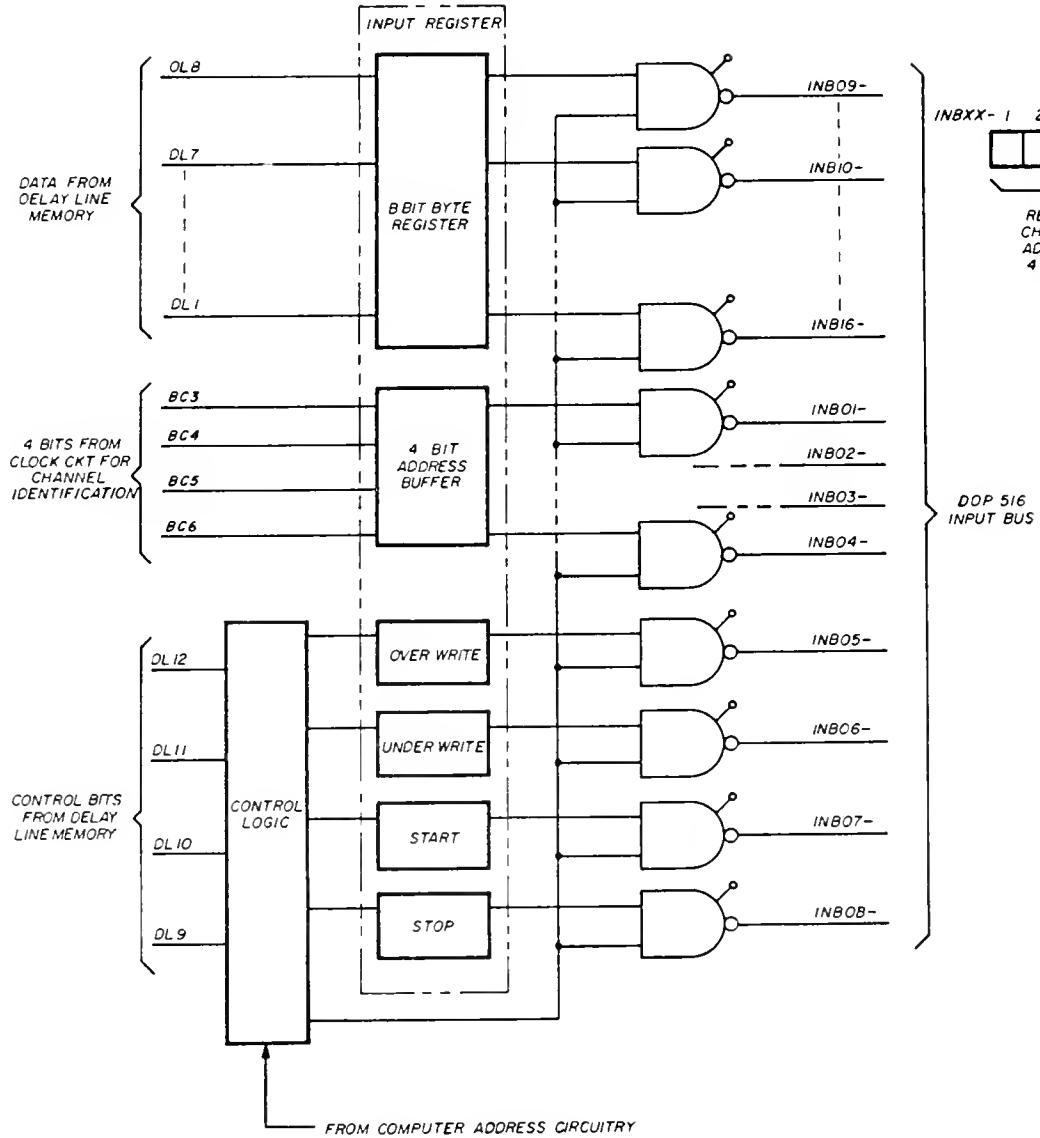
The output data register, which stores byte data with its corresponding 4-bit channel address, remains full until the appropriate cell in the delay line memory is addressed by using the address compare circuit--Fig. 9. Since the total cycle time of the memory is 64 μseconds, the byte data transfer to memory will take place within this time. When the output data register goes empty, it is ready to accept new computer output data.

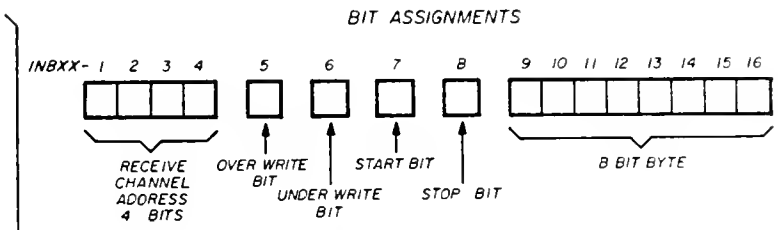
Interrupt Operation

There are two separate interrupts generated: one for all channels with receive byte data, and the other for all channels with transmit byte data. A real time clock is used to pace the interrupts.

The computer can then service the multiplexer in one routine for all transmitting channels, and one other routine for all receiving channels. This reduces the software overhead required for handling 16 serial data channels. The frequency of the interrupt

pacer must be selected to satisfy the byte level requirements of the serial channel with the highest bit rate.





FORMAT OF DATA ON INPUT BUS OF THE DDP 516

FIGURE B - 16 BIT INPUT REGISTER BUFFER

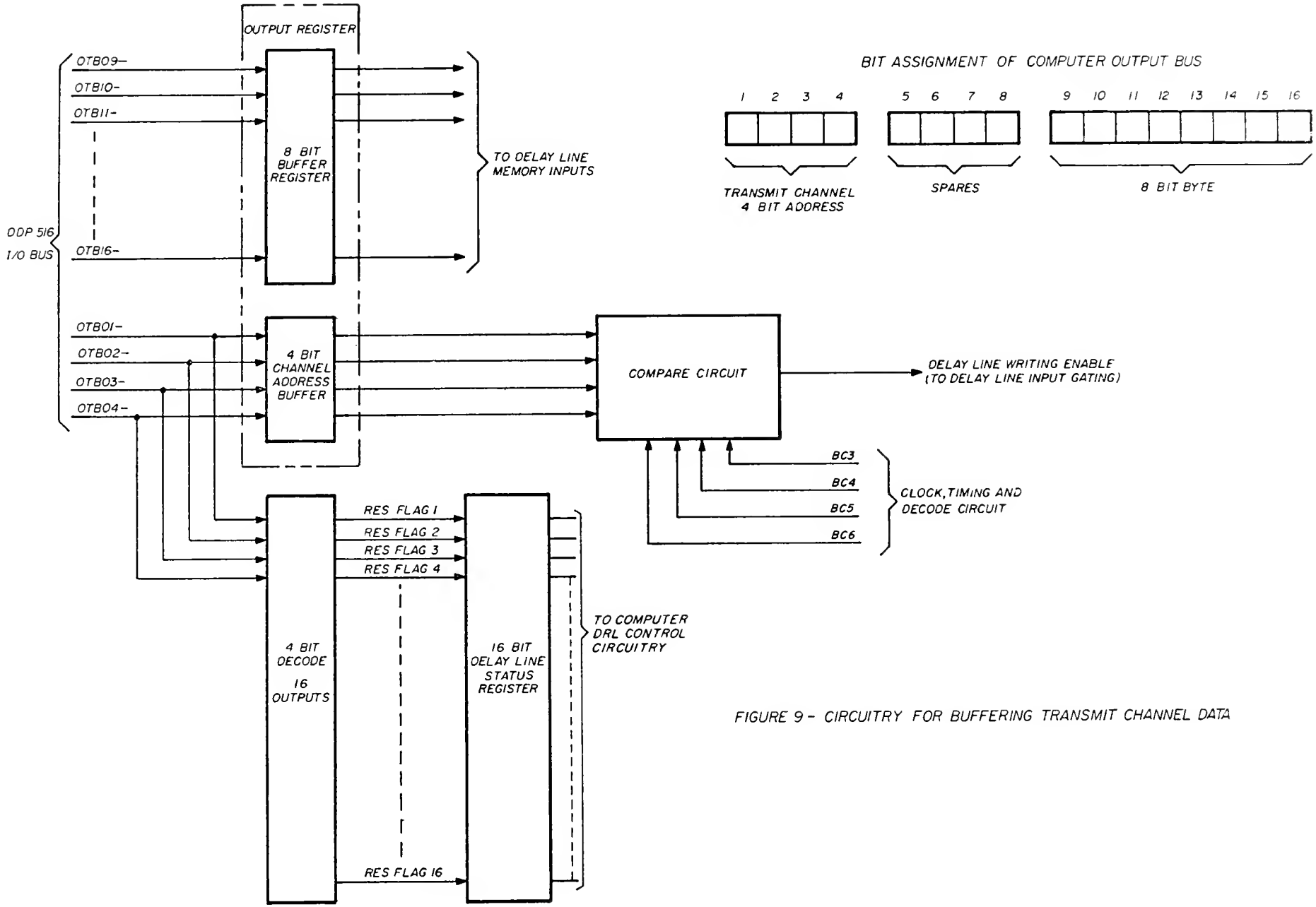


FIGURE 9 - CIRCUITRY FOR BUFFERING TRANSMIT CHANNEL DATA

4. SOFTWARE

4A. Software Specifications--Honeywell 16-Bit Series Machine

Interrupt Operation

SKS/430. Skip if not interrupting for input.

SKS/431. Skip if not interrupting for output.

SMK/020. Set mask for interrupting. A "1" in bit 3 of the A-register allows the multiplexer to interrupt for inputs. A "1" in bit 4 allows the multiplexer to interrupt for outputs. The master clear button on the computer console resets these bits.

Input Data to Computer

INA/1030. The program will skip the next instruction if the multiplexer is ready with data at the computer I/O bus. The next instruction is executed if the multiplexer is not ready to transfer data to the computer. The input data is in the format shown in Table III. Byte synchronization is performed in the multiplexer hardware. This feature can be bypassed on any individual channel if desired.

SKS/330. Skip if there are more inputs. If there are more inputs, the program may loop up to a maximum of 64 μseconds on the next INA/1030 instruction.

Outputing Data from the Computer to the Multiplexer

OTA/031. The program will skip the next instruction if the multiplexer accepts the output data. If it cannot accept the data,

the next instruction in the program is executed. The output data is in the format shown in Table IV. When the OTA/031 instruction is executed, the channel delay line byte buffer and the interface register of the multiplexer must be empty in order for the output data to be accepted.

SKS/331. Skip if there are any channel byte buffers empty.

SKS/231. Skip if the interface register is empty. The program may loop to a maximum of 64 μseconds, since the multiplexer hardware will empty the register within this time.

SKS/531. Specifying bits 1 through 4 of the output data format (Table IV) provides the test for the empty/full status of the channel delay line byte buffer. This instruction is a skip if empty.

Instructions for Setting Multiplexer Modes

OTA/131. This command unconditionally outputs a 16-bit word to the multiplexer. Bits 1 through 16 of the A-register represent channels 1 through 16. A "1" bit switches on the channel; a "0" bit switches off the channel. The master clear button on the computer console turns on all channels.

OTA/230. This command unconditionally outputs a 16-bit word to the multiplexer. Bits 1 through 16 of the A-register represent channels 1 through 16. A "1" bit sets the channel in the transmit mode; a "0" sets the channel in the receive mode. The master clear button on the computer console sets all channels to the receive mode.

INA/1130. This command unconditionally inputs a 16-bit word from the multiplexer. Bits 1 through 16 represent channels 1 through 16. A "1" bit indicates that a valid user is connected to the channel. A "0" bit indicates that there is no valid user connected to the channel.

Table III -- Input Data Format

Bits	Function
1 through 4	4-bit address.
5	Overwrite bit. A "1" bit indicates that the computer is not satisfying the channel input real time requirements.
6	Underwrite bit. A "1" bit indicates that the computer is not satisfying the channel output real time requirements.
7	Start bit. A "1" bit indicates the first byte of the receive message.
8	Stop bit. A "1" bit indicates that the channel has stop receiving.
9 through 16	8 bit receive byte.

Table IV -- Output Data Format

Bits	Function
1 through 4	4-bit channel address
5 through 8	Spare bits
9 through 16	8-bit transmit byte

4B. Computer I/O Examples

Multiplexer Input

The delay line memory is a sequential buffer which takes 64 μseconds to step through a complete cycle of memory. There is only one register between the delay line memory and the computer. If data can be accepted fast enough, the computer can do an effective scan of the delay line memory in 64 μseconds.

Straight line coding is an approach that can be used for an input scheme. In order that the computer completely scan the delay line memory for inputs, the three step input instruction set (DDP-516 computer) is repeated 22 times.

```
INPUT       BSZ  1
            INA  /1030
            JMP  *+2
            STA  BUFF 1
          ----------------
            INA  /1030
            JMP  *+2
            STA  BUFF 2
          ----------------
```

```
INA  /1030
JMP  *+2
STA  BUFF 3
------------------
     .
     .
     .
INA  /1030
JMP  *+2
STA  BUFF 22
JMP  * INPT
```

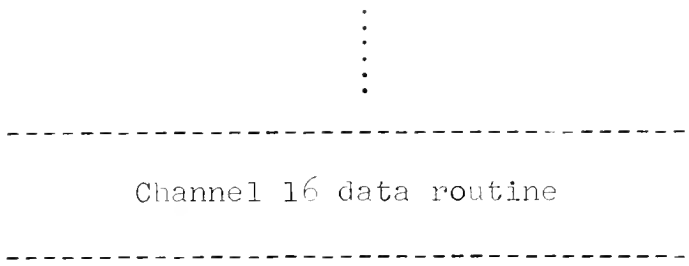
Multiplexer Output

When executing an OTA/031 instruction, the first 4 bits of the computer A-register specify which of the 16 channels the output data is for. In order for this instruction to be successfully executed, the output register (computer/multiplexer interface) and the byte static buffer (delay line memory) must be empty.

Again, as for inputing data to the computer, there is an access problem. With the first 4 bits in the A-register, the SKS/531 instruction can be used to check the status of the delay line memory for a given transmit channel. Since the computer will take 6.8 μseconds (DDP-516 computer) for each transmit channel output, data should not be outputed for two adjacent channels consecutively. This is because a word can be written into the delay line memory every 4 μseconds.

A program that can be used for outputing data to the multiplexer follows. It is continued until all channels that require output data have been tried.

```
OUT         BSZ  1
            LDA  Chan 1
            SKS  /531
            JMP  *+4
            OTA  /031
            JMP  *-1
            JMP  *+2
            STA  SAV 1
-----------------------------------
            LDA  Chan 3
            SKS  /531
            JMP  *+4
            ØTA  /031
            JMP  *-1
            JMP  *+2
            STA  SAV  3
-----------------------------------
     Channel 5 data routine
-----------------------------------
                 .
                 .
                 .
-----------------------------------
     Channel 15 data routine
-----------------------------------
     Channel 2 data routine
-----------------------------------
                 .
                 .
                 .
```


Channel 16 data routine

5. APPENDICES

Appendix A. RS-232-B Serial Channel Standard

The RS-232-B standard serial data channel is terminated by a 25 pin Cinch connector. Signals on the input and output pins are bi-polar DC levels: -6 volts or +6 volts. The connector pins and their corresponding channel functions are as follows:

Pin 1--Protective Ground (AA)

Pin 2--Transmitted Data (BA). The terminal supplies the NRZ data stream to this pin. A logical "1" is -6 volts. A logical "0" is +6 volts.

Pin 3--Received Data (BB). This pin outputs the NRZ data stream to the terminal. A logical "1" is -6 volts. A logical "0" is +6 volts.

Pin 4--Request to Send (CA). When transmitting data onto the channel, the terminal equipment must supply +6 volts to this pin. When receiving data from the channel, the terminal equipment must supply -6 volts to this pin.

Pin 5--Clear to send (CB). This pin supplies a +6 volt transmit enable signal to the terminal. A -6 volt signal will inhibit the terminal from transmitting. When a

terminal issues a CA signal to the channel, the channel will return, after a delay, a CB signal to the terminal.

Pin 6--Data Set Ready (CC). This pin supplies a +6 volt signal to the terminal to indicate when the channel can transmit or receive data. Ground indicates that the channel is not ready for communicating.

Pin 7--Signal Ground (AB).

Pin 8--Data Carrier Detector (CF). This pin supplies +6 volts to the terminal to indicate the presence of the Receive Clock (DD). -6 volts indicates the absence of DD.

Pin 9--Reserved for data set testing.

Pin 10-Reserved for data set testing.

Pin 11-Unassigned.

Pin 12-Unassigned.

Pin 13-Unassigned.

Pin 14-Unassigned.

Pin 15-Channel Transmit Clock (DB). This pin supplies a ±6 volt square wave to the terminal equipment when transmitting data into the channel. The positive transition of DB is used for shifting data on to the BA line from the terminal.

Pin 16-Unassigned.

Pin 17-Receiver Clock (DD). This pin supplies a ±6 volt square wave to the terminal equipment when receiving data from the channel. The BB line presents a new data bit at the

positive transition of DD.

Pin 18-Unassigned.

Pin 19-Unassigned.

Pin 20-Data Terminal Ready (CD). The terminal supplies +6 volts to this pin to indicate it is ready to operate. -6 volts indicates a not ready condition.

Pin 21-Unassigned.

Pin 22-Ring Indicator (CE). This pin supplies the terminal with +6 volts to indicate that there is a remote user trying to establish a communications link through the channel. Otherwise this pin is at -6 volts.

Pin 23-Unassigned.

Pin 24-External Transmit Clock (DA). The terminal supplies to this pin a ±6 volt square wave when the transmitted data through the channel is to be clocked by the terminal equipment.

Pin 25-Unassigned.

Appendix B. Honeywell 16-Bit Series Standard I/O Channel

The Honeywell 16-bit series standard I/O channel is a shared bus I/O system that consists basically of 48 twisted lead pairs. Thirty pairs are used for output and 18 pairs for input.

The 30 output twisted lead pairs are:

- 16-for data bits (OTBXX)
- 10-for address bits (ADBXX)
- 1-for reset ready (RRL)
- 1-for output command (OCP)
- 1-for master clear (MSTCL)
- 1-for set mask (SMSK)

The 18 input twisted lead pairs are:

- 16-for data bits (INBXX)
- 1-for device ready (DRL)
- 1-for program interrupt (PIL)

Signals on the output and input leads are DC levels: 0 or -6 volts in the DDP-116 and 0 or +6 volts in the DDP-416, DDP-516, and H-316. All leads are shared with all interfaces. Memory access I/O channels are available as options for all these 16-bit computers

The channel is synchronized by a specific time sequence of events. For example, within the I/O instructions there exist the following sequence of events: (a) an address goes out on the address bus, (b) a device decodes this address and responds, and (c) a strobe for the device terminates the instruction. The standard channel provides a hardware program interrupt feature to service devices on demand. The standard channel is a parallel I/O bus that is shared by all interfaces under program control.

The I/O software instructions and their hardware significance are discussed briefly.

Output Command (OCP)

This instruction initiates DC levels on the 10-bit address bus and a delay pulse on the output command twisted pair. This instruction is used to control the functioning of the I/O device, and expects no response from the device.

Sense Condition (SKS)

This instruction initiates DC levels on the 10-bit address bus and senses the input device ready lead. When a signal appears on this lead, during a set time in the instruction period, it causes the next instruction to be skipped. If no signal appears, the next instruction will be executed. This (SKS) instruction is used to test conditions of specific interfaces on the I/O bus.

Single Word Input (INA)

The input instruction initiates action by placing DC levels on the 10-bit address bus. The addressed interface then places its input data on the 16-bit input bus; simultaneously, a signal is placed on the input device ready lead. The computer will acknowledge the input with a signal on the output reset ready lead, and will skip the next instruction to be executed. In the event of no input, the addressed interface does not return a device ready signal. The computer does not skip the next instruction, nor acknowledge an input with a signal on the reset ready lead. Multiple word inputs must be accomplished by creating a program loop of single word (INA) inputs.

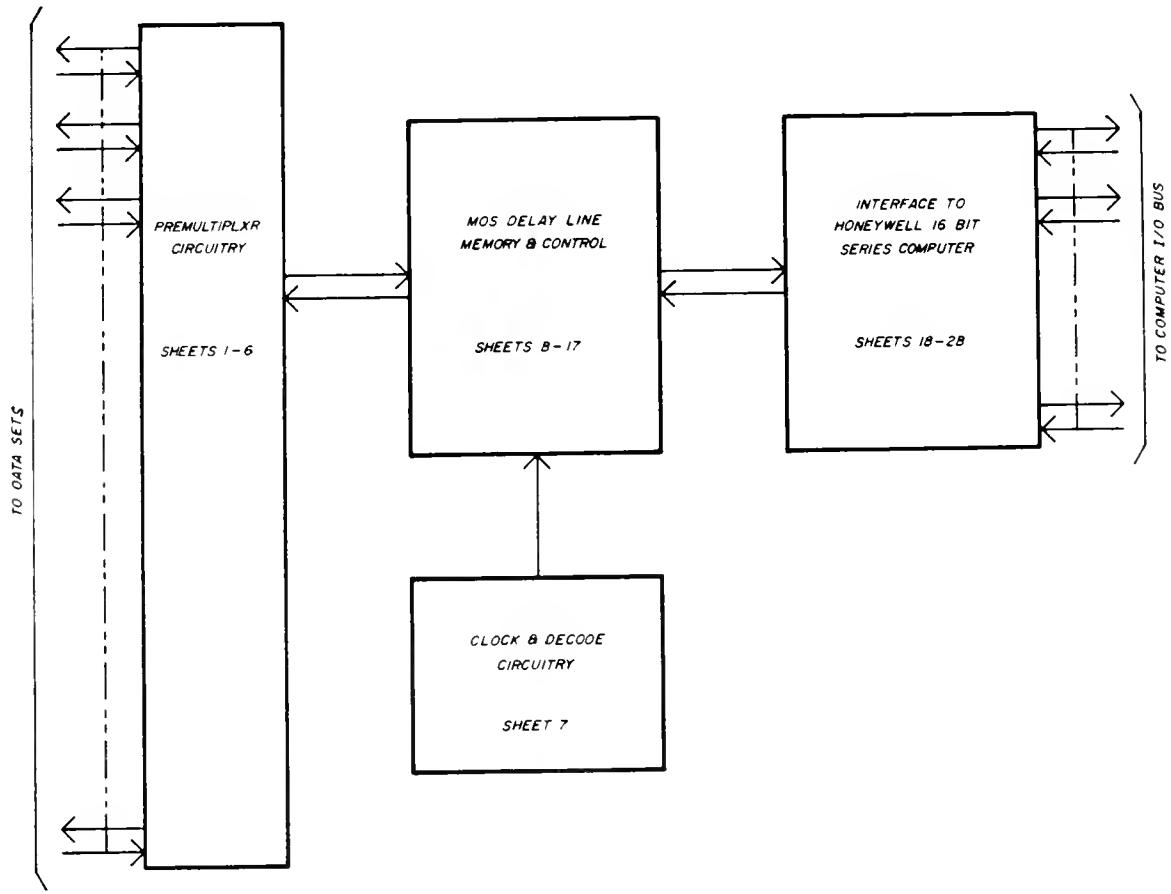
Single Word Output (ØTA)

The output instruction initiates action by placing DC levels on the 10-bit address bus and the 16-bit output bus. The addressed interface accepts the data by placing a signal on the input device ready lead. The computer will then respond on the reset ready lead with a signal which can be used as a strobe for the output data. The computer will then skip the next instruction to be executed. In the event the addressed interface does not accept the output, the computer will not skip the next instruction, nor respond with a signal on the reset ready lead. Multiple word outputs must be accomplished by creating a program loop of single word (ØTA) outputs.

Any interface on the I/O bus can initiate an interrupt by placing a DC level on the program interrupt lead (PIL). Since this lead is common to all interfaces, when an interrupt occurs a program using the sense condition instruction (SKS) must be used to seek out the source of interrupt, and then jump to a subroutine to service it. Priorities of program interrupts are accomplished through the use of mask bits. Each interface is assigned a bit which is used to generate its program interrupt (PIL) signal.

Refer to Honeywell Interface Manual (Pub. No. 130071624) for further details on the I/O channel of the 16-bit series computers.

Appendix C. System Schematics



INDEX

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	ENGINEERING RESEARCH LABORATORY
ENG V.P.	DR BY A.M.K. DATE 7-10-70
DRAWING NO 540	SHEET NO COVER
TITLE	16 PORT DATA SET MULTIPLXR

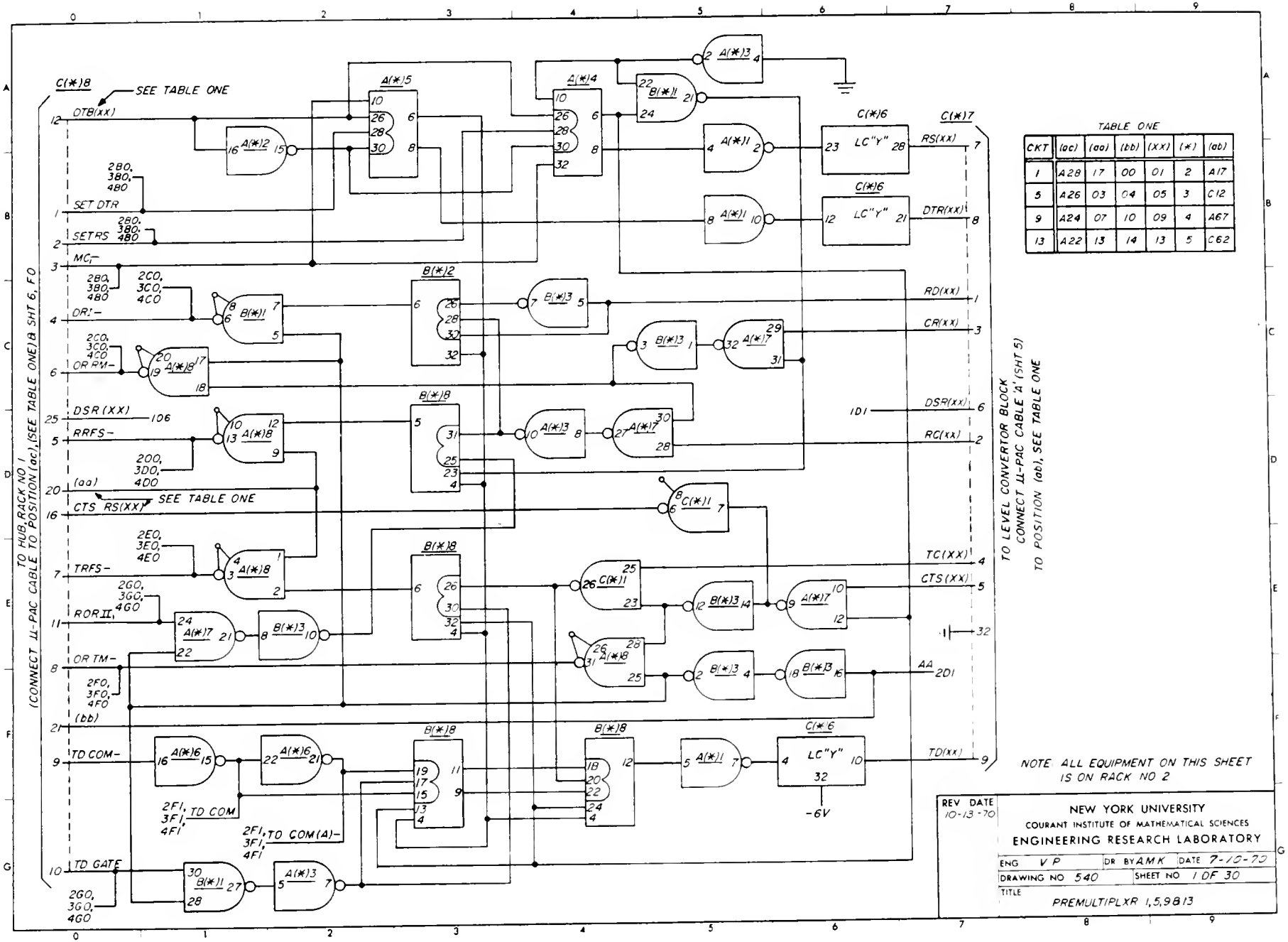

TABLE ONE

CKT	(ac)	(aa)	(bb)	(XX)	(*)	(ab)
1	A28	17	00	01	2	A17
5	A26	03	04	05	3	C12
9	A24	07	10	09	4	A67
13	A22	13	14	13	5	C62

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ENG	V P	DR BY AMK	DATE 7-10-70
DRAWING NO	540	SHEET NO	1 OF 30

TITLE
PREMULTIPLXR 1,5,9 B 13

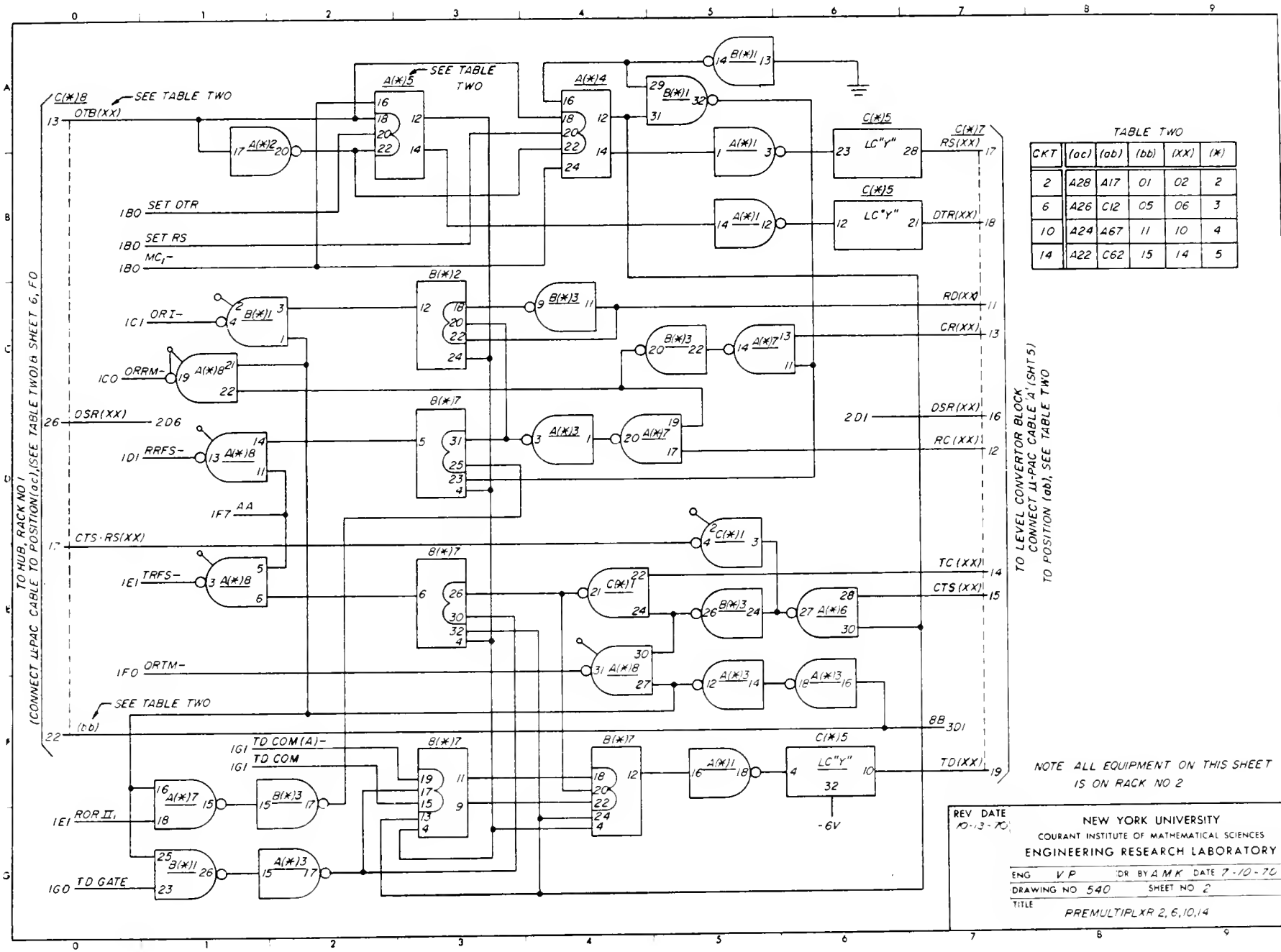

TABLE TWO

CKT	(ac)	(ab)	(bb)	(XX)	(*)
2	A28	A17	01	02	2
6	A26	C12	05	06	3
10	A24	A67	11	10	4
14	A22	C62	15	14	5

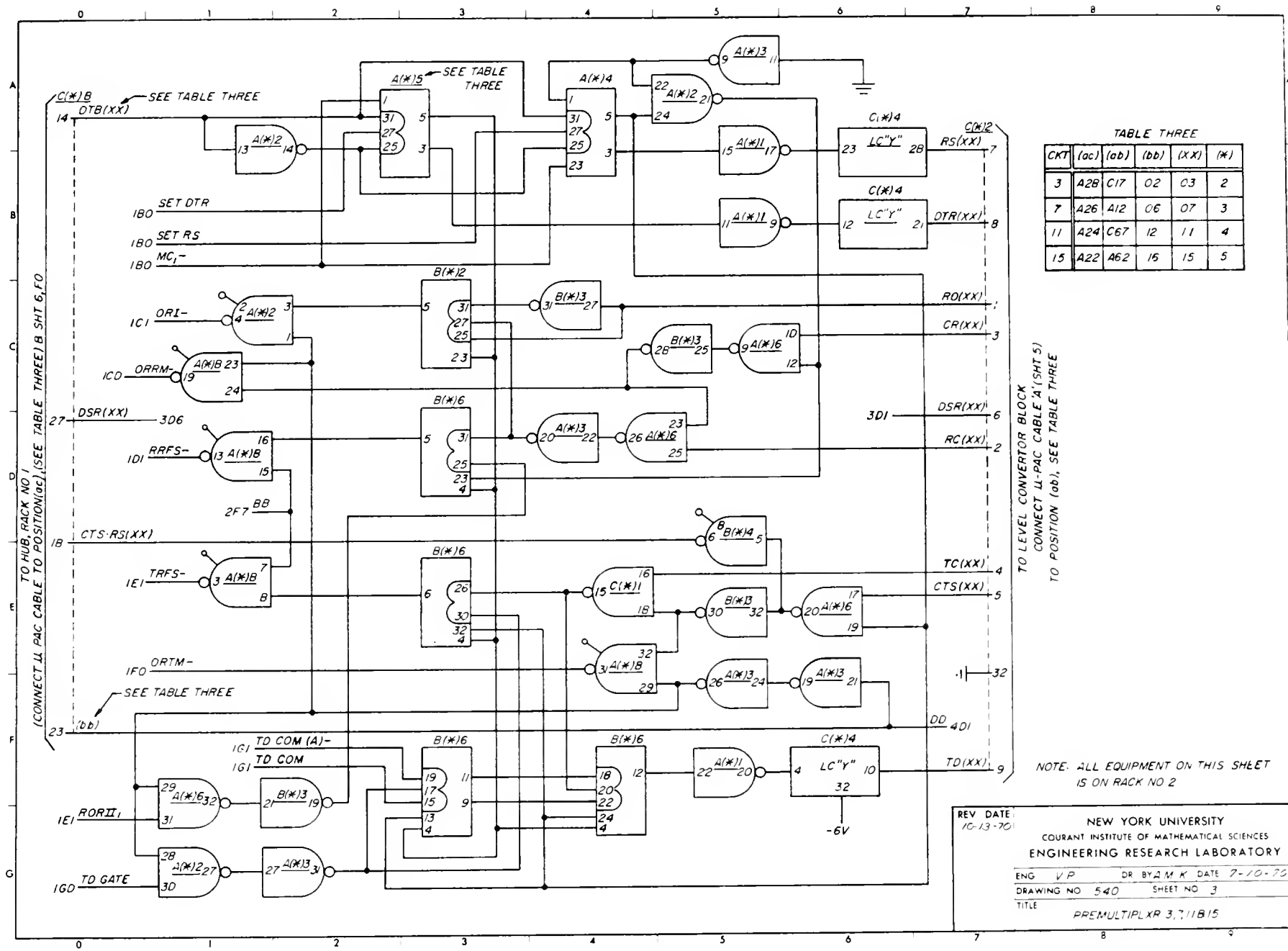

TABLE THREE

CKT	(ac)	(ab)	(bb)	(XX)	(*)
3	A28	C17	02	03	2
7	A26	A12	06	07	3
11	A24	C67	12	11	4
15	A22	A62	15	15	5

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ENG V P DR BY A M K DATE 7-10-70
DRAWING NO 540 SHEET NO 3
TITLE PREMULTIPLXR 3,7,11,15

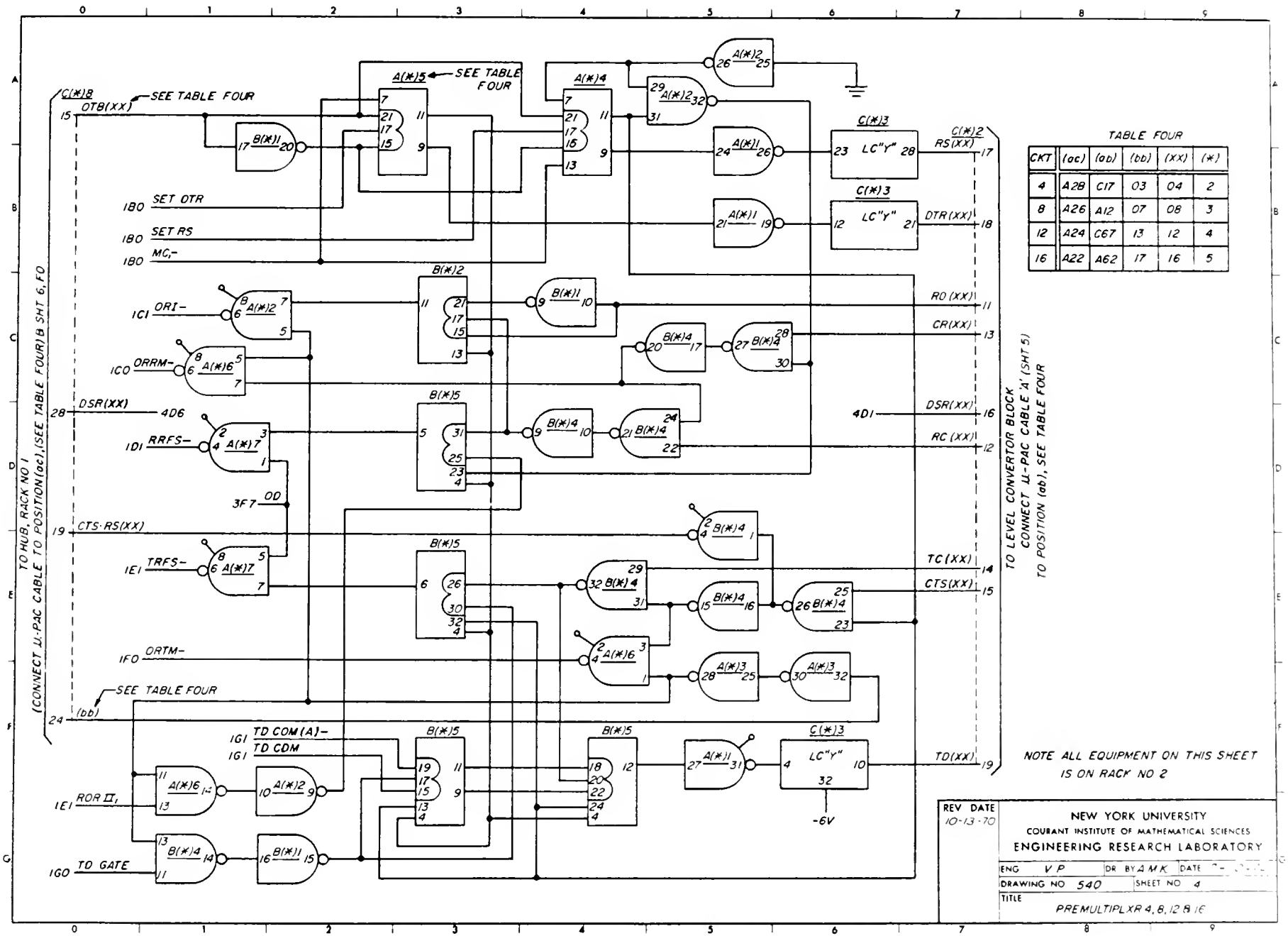
TABLE FOUR
CKT | (ac) | (ab) | (bb) | (XX) | (*)
4 | A28 | C17 | 03 | 04 | 2
8 | A26 | A12 | 07 | 08 | 3
12 | A24 | C67 | 13 | 12 | 4
16 | A22 | A62 | 17 | 16 | 5
TO HUB, RACK NO 1
(CONNECT U-PAC CABLE TO POSITION (ac), (SEE TABLE FOUR) B SHT 6, F0
TO LEVEL CONVERTOR BLOCK
CONNECT U-PAC CABLE 'A' (SHT 5)
TO POSITION (ab), SEE TABLE FOUR
NOTE ALL EQUIPMENT ON THIS SHEET IS ON RACK NO 2
-6V
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ENG V P
DR BY A M K
DRAWING NO 540
SHEET NO 4
TITLE
PREMULTIPLXR 4, 8, 12 & 16

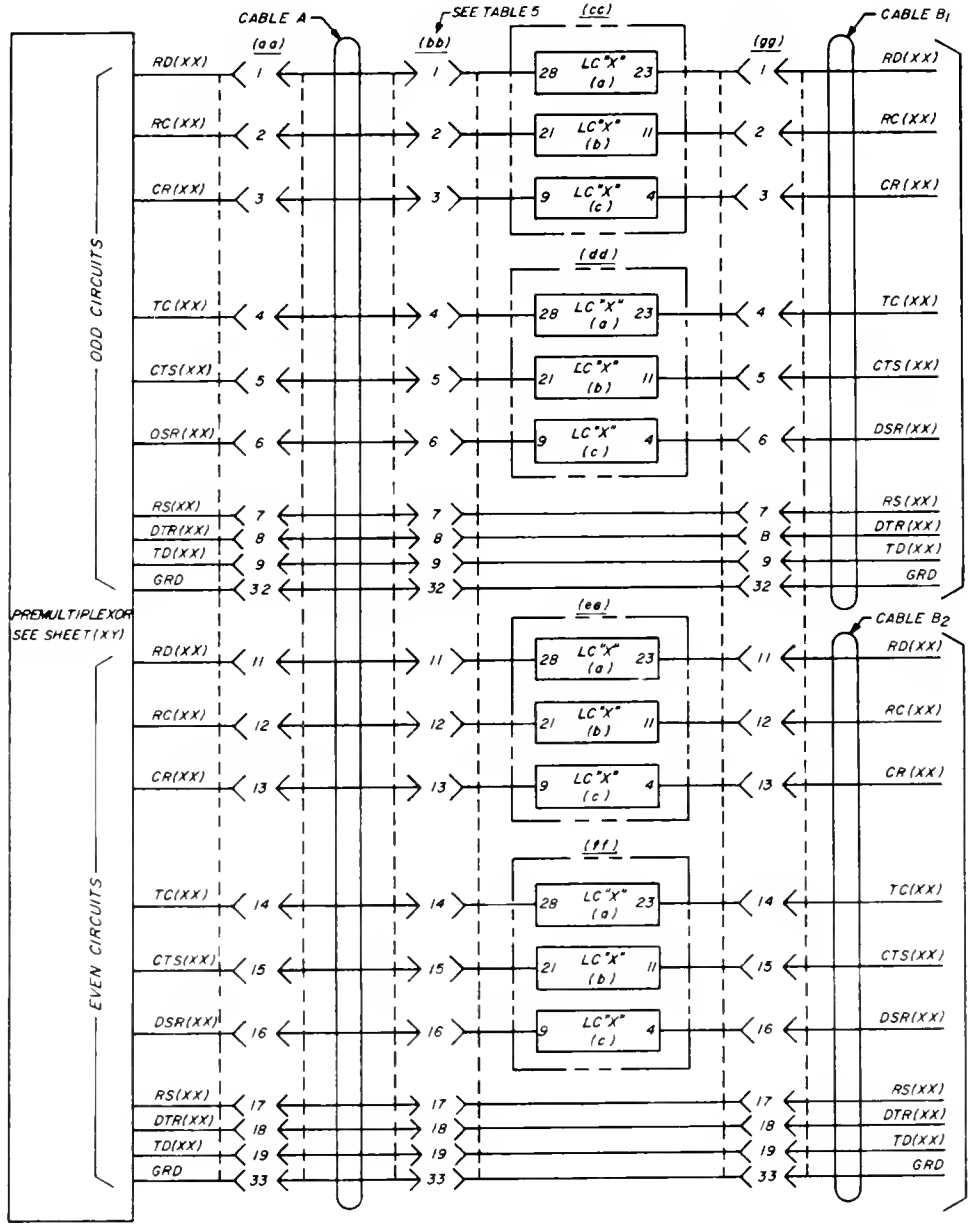
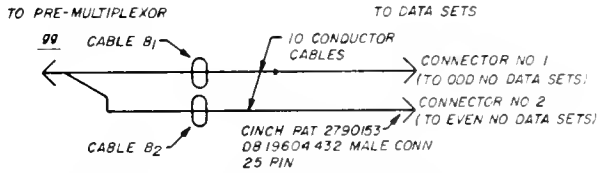


TABLE FIVE

DATA SET	(XX)	(XY)	(aa)	(bb)	(cc)	(dd)	(ee)	(ff)	(gg)	(hh)	(jj)
1	01	1	C27	A17	A16	A15	–	–	A18	–	1
2	02	2	C27	A17	–	–	B18	B17	A18	2	–
3	03	3	C22	C17	C16	C15	–	–	C18	–	3
4	04	4	C22	C17	–	–	B16	B15	C18	4	–
5	05	1	C37	C12	C13	C14	–	–	C11	–	5
6	06	2	C37	C12	–	–	B13	B14	C11	6	–
7	07	3	C32	A12	A13	A14	–	–	A11	–	7
8	08	4	C32	A12	–	–	B11	B12	A11	8	–
9	09	1	C47	A67	A66	A65	–	–	A68	–	9
10	10	2	C47	A67	–	–	B68	B67	A68	10	–
11	11	3	C42	C67	C66	C65	–	–	C68	–	11
12	12	4	C42	C67	–	–	B66	B65	C68	12	–
13	13	1	C57	C62	C63	C64	–	–	C61	–	13
14	14	2	C57	C62	–	–	B63	B64	C61	14	–
15	15	3	C52	A62	A63	A64	–	–	A61	–	15
16	16	4	C52	A62	–	–	B61	B62	A61	16	–



TERM NO U-PAC	SIGNAL		DATA SET CONN	
1	TO ODD NO DATA SETS	RD__	CONN NO 1	3
2		RC__		17
3		CR__		8
4		TC__		15
5		CTS__		5
6		DSR__		6
7		RS__		4
8		DTR__		20
9		TD__		2
32		GRD		7 (STRAP 7B11)
11	TO EVEN NO DATA SETS	RD__	CONN NO. 2	3
12		RC__		17
13		CR__		8
14		TC__		15
15		CTS__		5
16		DSR__		6
17		RS__		4
18		DTR__		20
19		TD__		2
33		GRD		7 (STRAP 7B11)

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ENG V P	DR BY A M K	DATE 7-10-70
DRAWING NO 540	SHEET NO 5	

TITLE: PREMULTIPLXR TO DATA SET CABLING

TABLE 6

'A'6 PRE-MULT LOCATION	'B'6 SIGNAL	'C'6 PIN NO	'D'6 HUB LOCATION
		35	
		34	
		33	
		32	
		31	
		30	
		29	
4D0	DSR 16	28	23F4
3D0	DSR 15	27	23E4
2D0	DSR 14	26	23E4
1D0	DSR 13	25	23D4
4F0	17	24	7C9
3F0	16	23	7C9
2F0	15	22	7C9
1F7	14	21	7B9
1D0	13	20	7B9
4D0	CTSRS16	19	26G4
3D0	CTSRS15	18	26E4
2D0	CTSRS14	17	26D4
1D0	CTSRS13	16	26B4
4A0	OTBI6	15	27D0
3A0	OTBI5	14	27D1
2A0	OTBI4	13	27D1
1A0	OTBI3	12	27D2
1E0	ROR II$_1$	11	8D9
1G0	TO GATE	10	8C9
1F0	TD COM-	9	8F9
1F0	ORTM-	8	8B0
1E0	TRFS-	7	8F0
1C0	ORRM-	6	8A0
1D0	RRFS-	5	8E0
1C0	ORI-	4	8G0
1B0	MC$_1$-	3	22D0
1B0	SET RS	2	21C9
1B0	SET DTR	1	21B9

TABLE 7

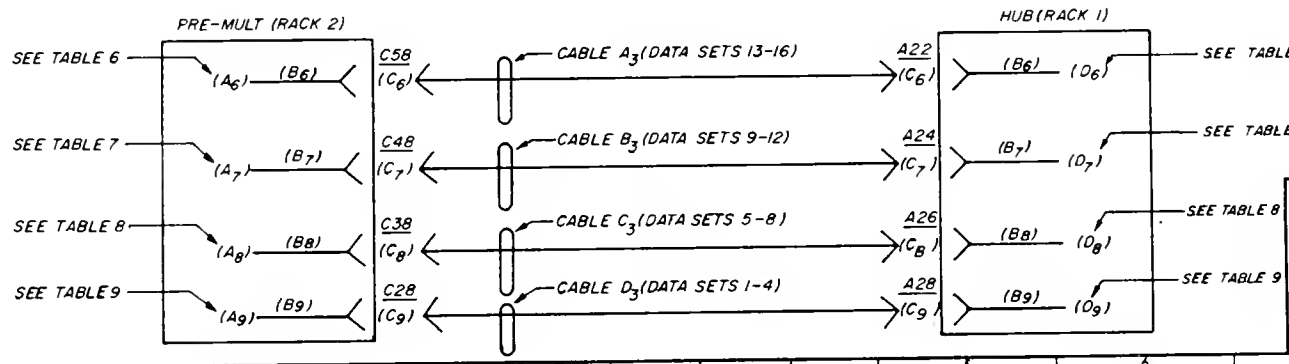
'A'7 PRE-MULT LOCATION	'B'7 SIGNAL	'C'7 PIN NO	'D'7 HUB LOCATION
		35	
		34	
		33	
		32	
		31	
		30	
		29	
4D0	DSR 12	28	23C4
3D0	DSR11	27	23C4
2D0	DSR10	26	2384
1D0	DSR09	25	23B4
4F0	13	24	7B9
3F0	12	23	7B9
2F0	11	22	7A9
1F7	10	21	7A9
1D0	07	20	7F9
4D0	CTS RS12	19	26G0
3D0	CTSRS11	18	26E0
2D0	CTSRS10	17	26D0
1D0	CTSRS09	16	26B0
4A0	OTBI2	15	27D3
3A0	OTBI1	14	27D3
2A0	OTBI0	13	27D4
1A0	OTB09	12	27D4
1E0	ROR II$_1$	11	8D9
1G0	TD GATE	10	8C9
1F0	TD COM-	9	8F9
1F0	ORTM-	8	8B0
1E0	TRFS-	7	8F0
1C0	ORRM-	6	8A0
1D0	RRFS-	5	8E0
1C0	ORI-	4	8G0
1B0	MC$_1$-	3	22D0
1B0	SET RS	2	21C9
1B0	SET DTR	1	21B9

TABLE 8

'A'8 PRE-MULT LOCATION	'B'8 SIGNAL	'C'8 PIN NO	'D'8 HUB LOCATION
		35	
		34	
		33	
		32	
		31	
		30	
		29	
4D0	DSR 08	28	23F1
3D0	DSR 07	27	23E1
2D0	DSR 06	26	23D1
1D0	DSR 05	25	23D1
4F0	07	24	7F9
3F0	06	23	7F9
2F0	05	22	7F9
1F7	04	21	7E9
1D0	03	20	7E9
4D0	CTSRS 08	19	25G4
3D0	CTSRS 07	18	25E4
2D0	CTSRS 06	17	25D4
1D0	CTSRS 05	16	25B4
4A0	OTB08	15	27D5
3A0	OTB07	14	27D5
2A0	OTB06	13	27D6
1A0	OTB05	12	27D7
1E0	ROR II$_1$	11	8D9
1G0	TD GATE	10	8C9
1F0	TD COM-	9	8F9
1F0	ORTM-	8	8B0
1E0	TRFS-	7	8F0
1C0	ORRM-	6	8A0
1D0	RRFS-	5	8E0
1C0	ORI-	4	8G0
1B0	MC$_1$-	3	22D0
1B0	SET RS	2	21C9
1B0	SET DTR	1	21B9

TABLE 9

'A'9 PRE-MULT LOCATION	'B'9 SIGNAL	'C'9 PIN NO	'D'9 HUB LOCATION
		35	
		34	
		33	
		32	
		31	
		30	
		29	
4D0	DSR 04	28	23C1
3D0	DSR03	27	23C1
2D0	DSR 02	26	23B1
1D0	DSR01	25	23B1
4F0	03	24	7E9
3F0	02	23	7E9
2F0	01	22	709
1F7	00	21	709
1D0	17	20	7C9
4D0	CTS RS 04	19	25G0
3D0	CTSRS 03	18	25E0
2D0	CTSRS 02	17	2500
1D0	CTSRS 01	16	2580
4A0	OTB04	15	27D7
3A0	OTB03	14	27D8
2A0	OTB02	13	27D8
1A0	OTB01	12	27D9
1E0	ROR II$_1$	11	8D9
1G0	TD GATE	10	8C9
1F0	TD COM-	9	8F9
1F0	ORTM-	8	8B0
1E0	TRFS-	7	8F0
1C0	ORRM-	6	8A0
1D0	RRFS-	5	8E0
1C0	ORI-	4	8G0
1B0	MC$_1$-	3	22D0
1B0	SET RS	2	21C9
1B0	SET DTR	1	21B9



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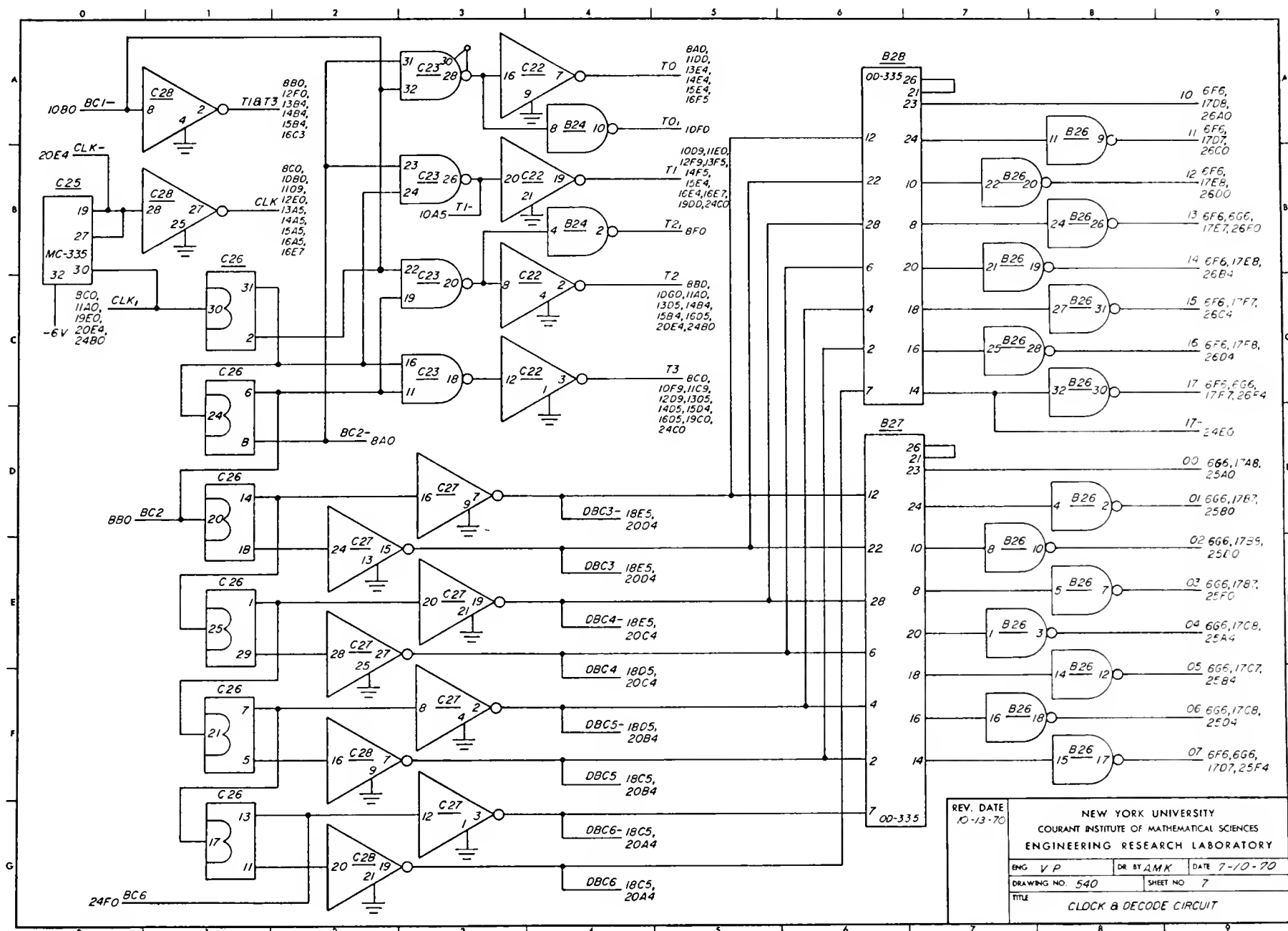
	ENG VP · DR. BY AMK · DATE 7-10-70
	DRAWING NO 540 · SHEET NO. 6
	TITLE: HUB TO PREMULTIPLXR CABLING


BC1-
1080
C28
T1&T3
8B0, 12F0, 13B4, 14B4, 15B4, 16C3
CLK-
20E4
C25
MC-335
CLK
8C0, 1DB0, 1109, 12E0, 13A5, 14A5, 15A5, 16A5, 16E7
CLK1
8C0, 11A0, 19E0, 20E4, 24B0
-6V
C26
C23
C22
B24
T0
8A0, 11D0, 13E4, 14E4, 15E4, 16F5
T0-
10F0
T1
1009, 11E0, 12F9, 13F5, 14F5, 15E4, 16E4, 16E7, 19D0, 24C0
10A5
T1-
T2-
8F0
T2
8B0, 10G0, 11A0, 13D5, 14B4, 15B4, 16D5, 20E4, 24B0
T3
8C0, 10F9, 11C9, 12D9, 13D5, 14D5, 15D4, 16D5, 19C0, 24C0
BC2-
8A0
BC2
BB0
C27
C28
DBC3-
18E5, 2004
DBC3
18E5, 2004
DBC4-
18E5, 20C4
DBC4
18D5, 20C4
DBC5-
18D5, 20B4
DBC5
18C5, 20B4
DBC6-
18C5, 20A4
DBC6
18C5, 20A4
BC6
24F0
B28
00-335
B26
10 6F6, 17D8, 26A0
11 6F6, 17D7, 26C0
12 6F6, 17E8, 26D0
13 6F6, 6G6, 17E7, 26F0
14 6F6, 17E8, 26B4
15 6F6, 17F7, 26C4
16 6F6, 17F8, 26D4
17 6F8, 6G6, 17F7, 26E4
17- 24E0
B27
00 6G6, 17A8, 25A0
01 6G6, 17B7, 25B0
02 6G6, 17B8, 25C0
03 6G6, 17B7, 25F0
04 6G6, 17C8, 25A4
05 6G6, 17C7, 25B4
06 6G6, 17C8, 25D4
07 6F6, 6G6, 17D7, 25F4
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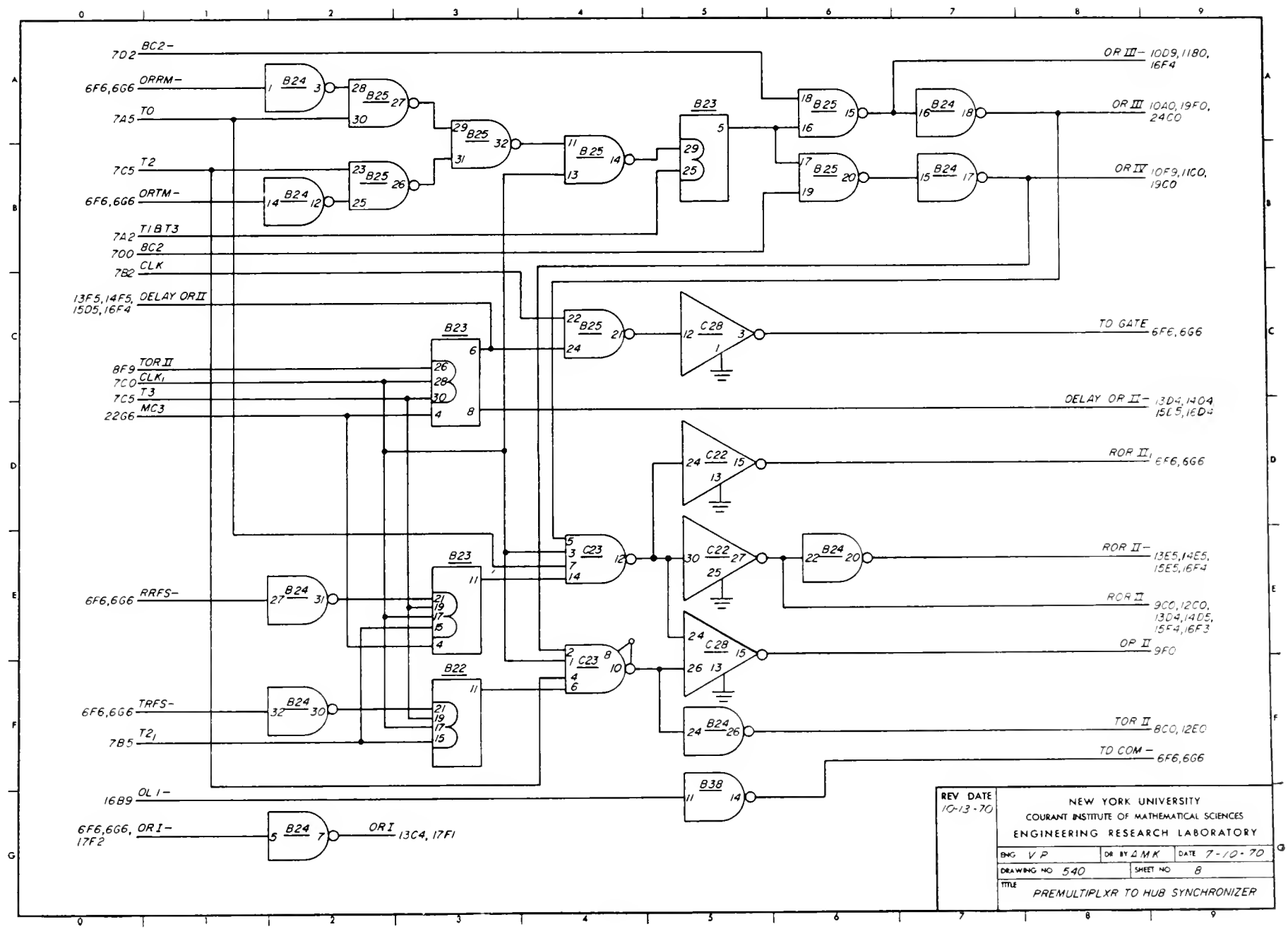
ENG V P
DR BY AMK
DATE 7-10-70
DRAWING NO. 540
SHEET NO 7
TITLE
CLOCK & DECODE CIRCUIT


7D2 BC2-
6F6,6G6 ORRM-
7A5 TO
7C5 T2
6F6,6G6 ORTM-
7A2 T1 B T3
700 BC2
7B2 CLK
13F5,14F5, 15D5,16F4 DELAY OR II
8F9 TOR II
7C0 CLK1
7C5 T3
22G6 MC3
6F6,6G6 RRFS-
6F6,6G6 TRFS-
7B5 T21
16B9 OL1-
6F6,6G6, 17F2 ORI-
ORI 13C4, 17F1
OR III- 10D9, 11B0, 16F4
OR III 10A0, 19F0, 24C0
OR IV 10F9, 11C0, 19C0
TO GATE 6F6, 6G6
DELAY OR II- 13D4, 14D4 15D5, 16D4
ROR II1 6F6, 6G6
ROR II- 13E5, 14E5, 15E5, 16F4
ROR II 9C0, 12C0, 13D4, 14D5, 15F4, 16F3
OR II 9F0
TOR II 8C0, 12E0
TO COM- 6F6, 6G6
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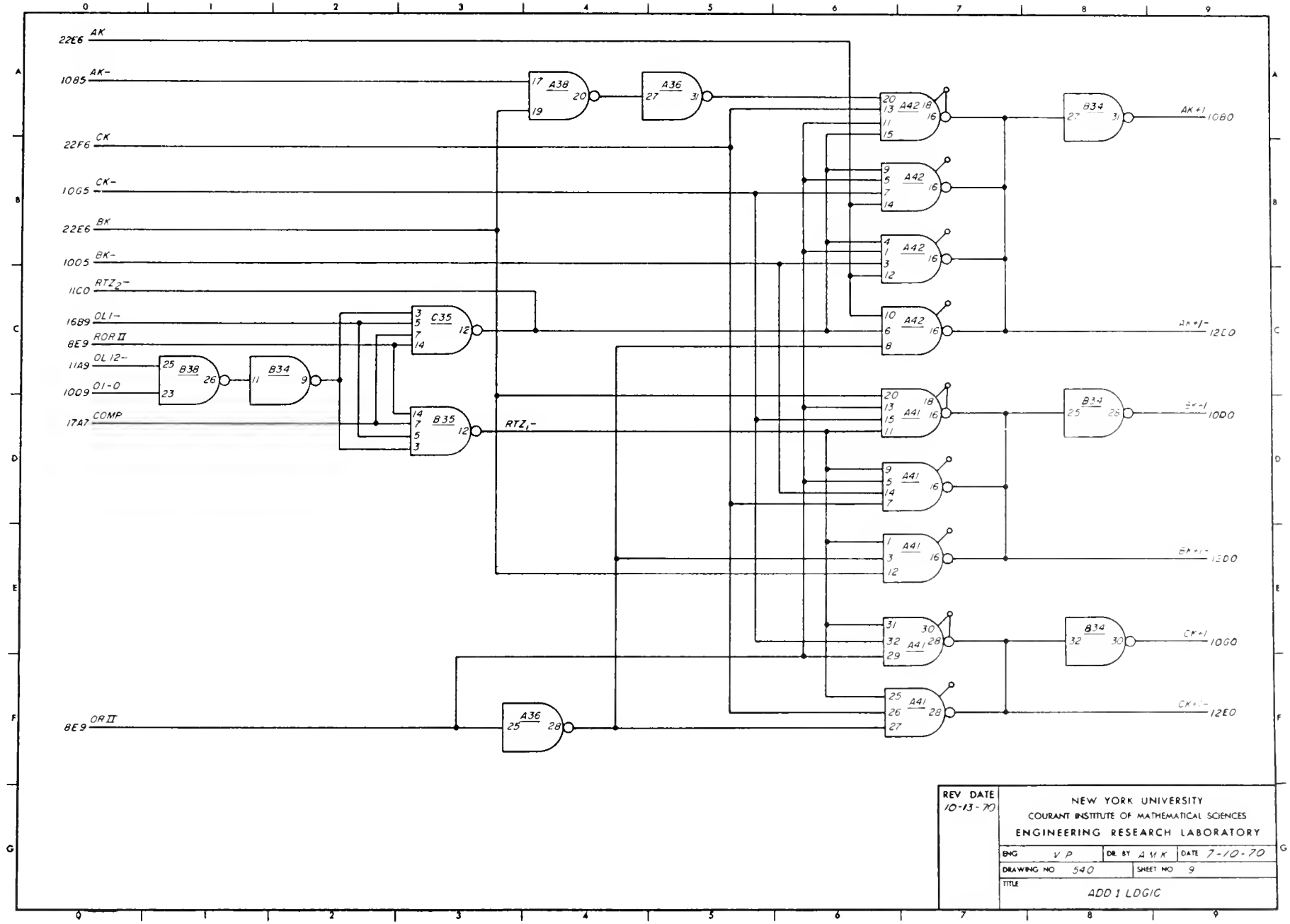
ENG V P
DR BY A M K
DATE 7-10-70
DRAWING NO 540
SHEET NO 8
TITLE PREMULTIPLXR TO HUB SYNCHRONIZER



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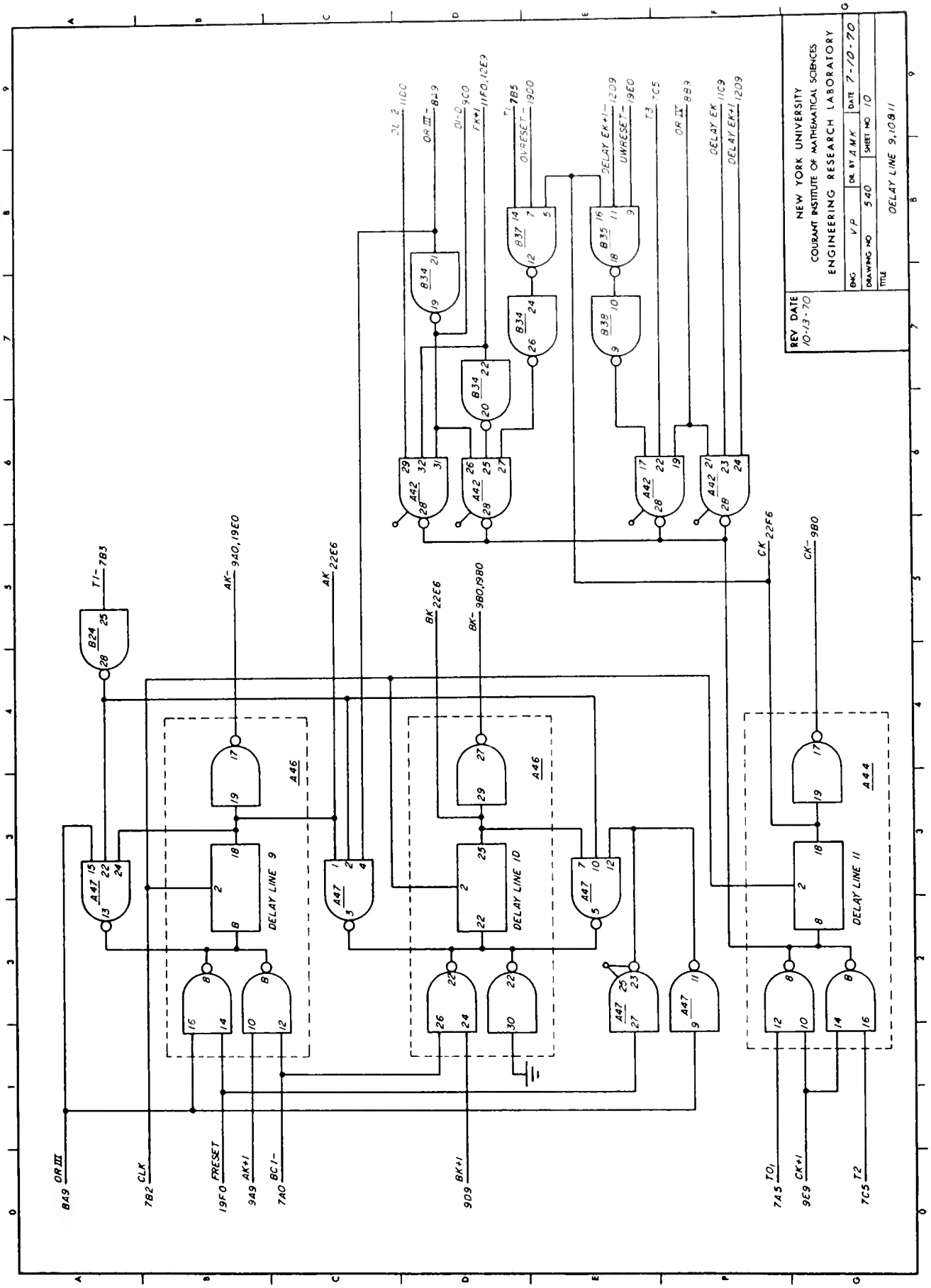
DRAWING NO 540	SHEET NO 9
TITLE	ADD 1 LOGIC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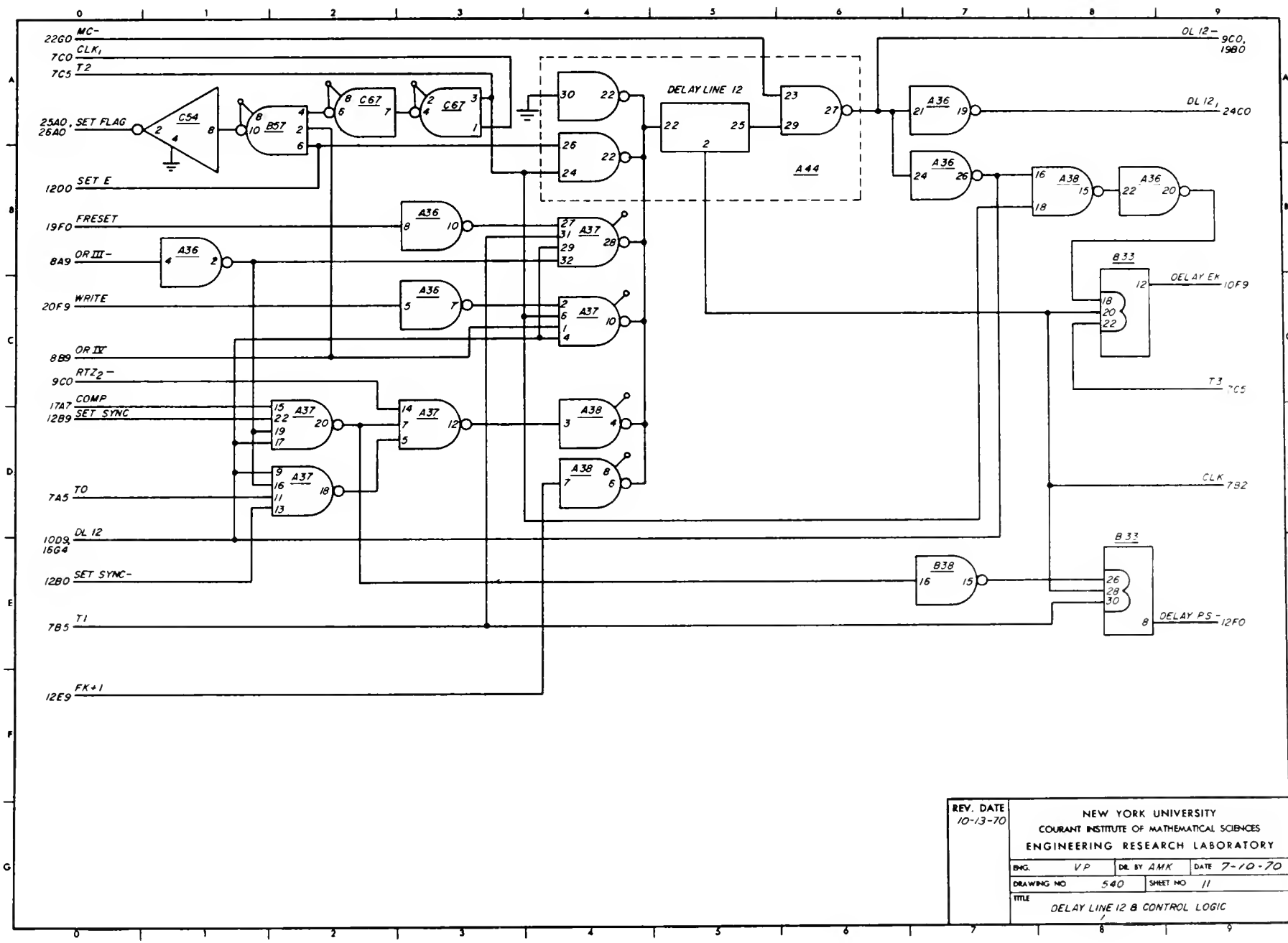
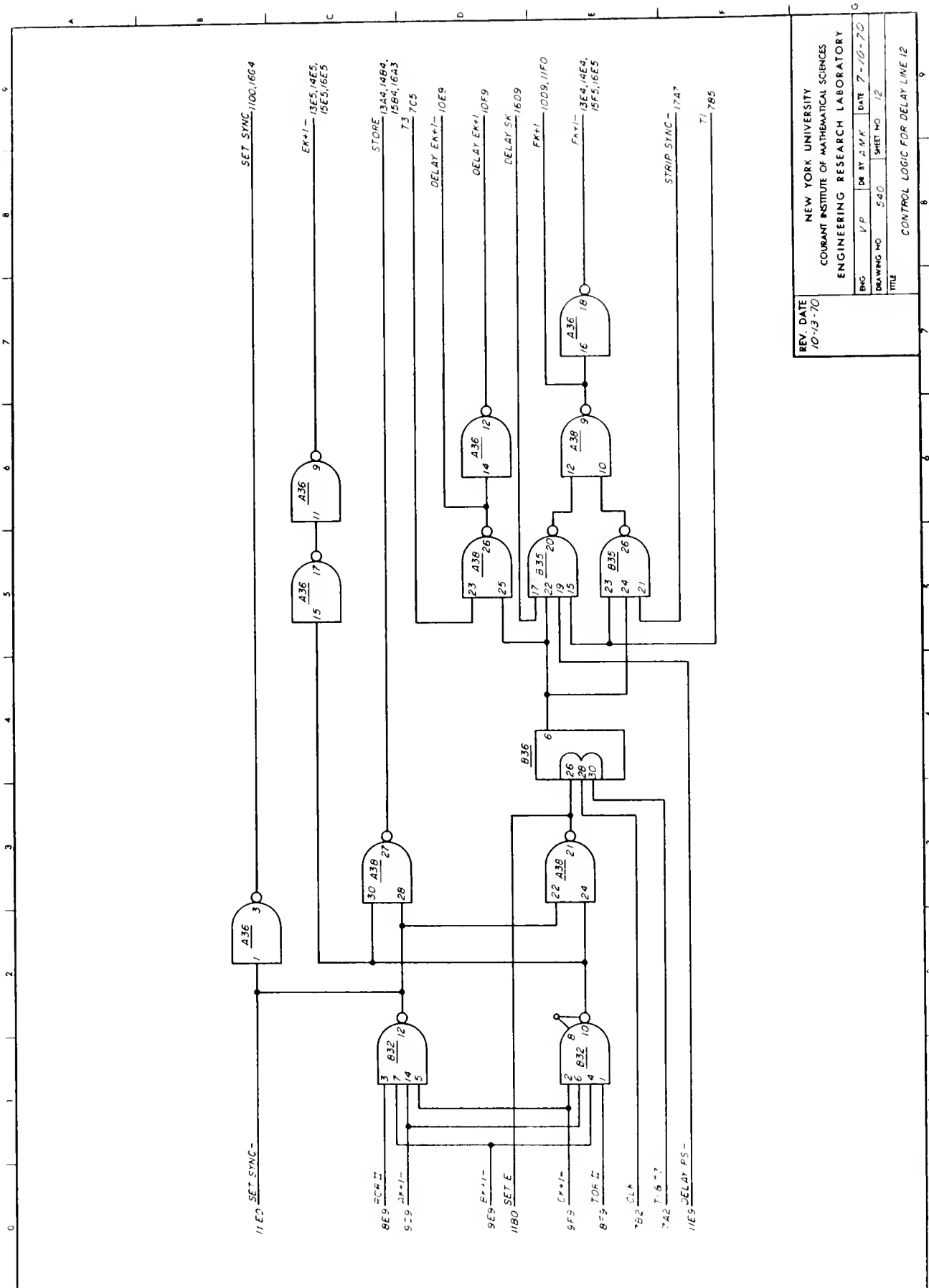
DRG VP
DR BY A MK
DATE 7-10-70
DRAWING NO 540
SHEET NO 10
TITLE DELAY LINE 9,10 & 11
REV DATE 10-13-70
DELAY LINE 9
DELAY LINE 10
DELAY LINE 11
A46
A44
B24
A47
B34
B37
B35
B38
A42
OR III
CLK
PRESET
AK+1
BC1-
BK+1
CK+1
T1
T2
AK- 940,19E0
AK 22E6
BK 22E6
BK- 980,19B0
CK 22F6
CK- 980
T1- 783
T1 785
OR III- 849
OR IV 889
T3 7C5
DELAY EK 1109
DELAY EK+1 1209
DELAY EK+1- 1209
UNRESET- 19E0
OVRESET- 1900
FK+1 11F0,12E9
OL 2 11DC
OL-D 9C0



REV. DATE 10-13-70	NEW YORK UNIVERSITY COURANT INSTITUTE OF MATHEMATICAL SCIENCES ENGINEERING RESEARCH LABORATORY		
	ENG. VP	DR. BY AMK	DATE 7-10-70
	DRAWING NO 540	SHEET NO 11	
	TITLE DELAY LINE 12 & CONTROL LOGIC		


SET SYNC 1100,1664
EK+/- 13E5,14E5, 15E5,16E5
STORE 13A4,14B4, 15B4,16A3
7C5
DELAY EK+/- 10E9
DELAY EK+1 10F9
DELAY SK 16D9
FK+1 1009,11F0
FK+/- 13E4,14E4, 15F5,16E5
STRIP SYNC- 17A7
T1 7B5
A36
A38
B35
B36
B32
SET SYNC-
SET E
DELAY PS-
NEW YORK UNIVERSITY
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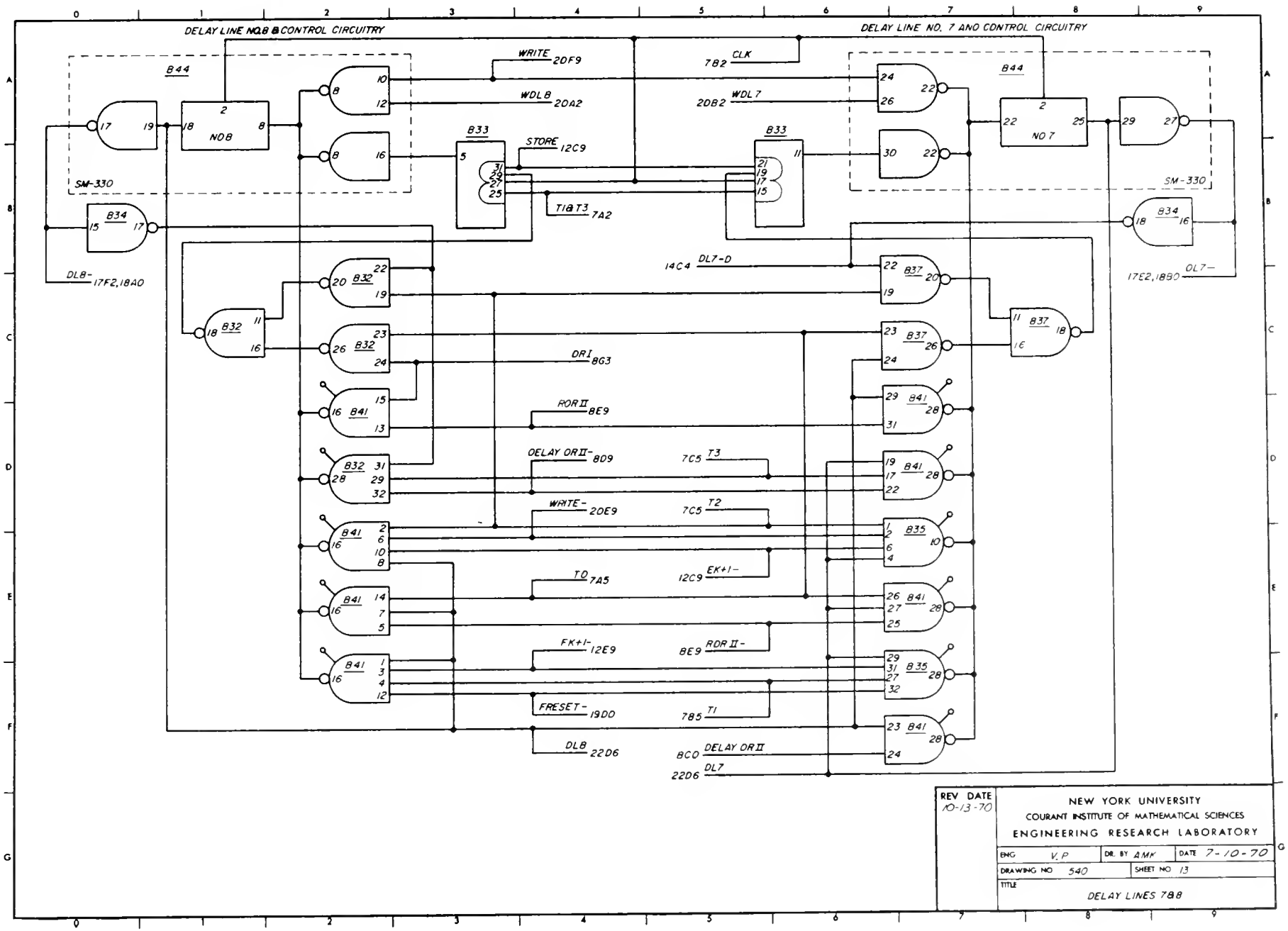
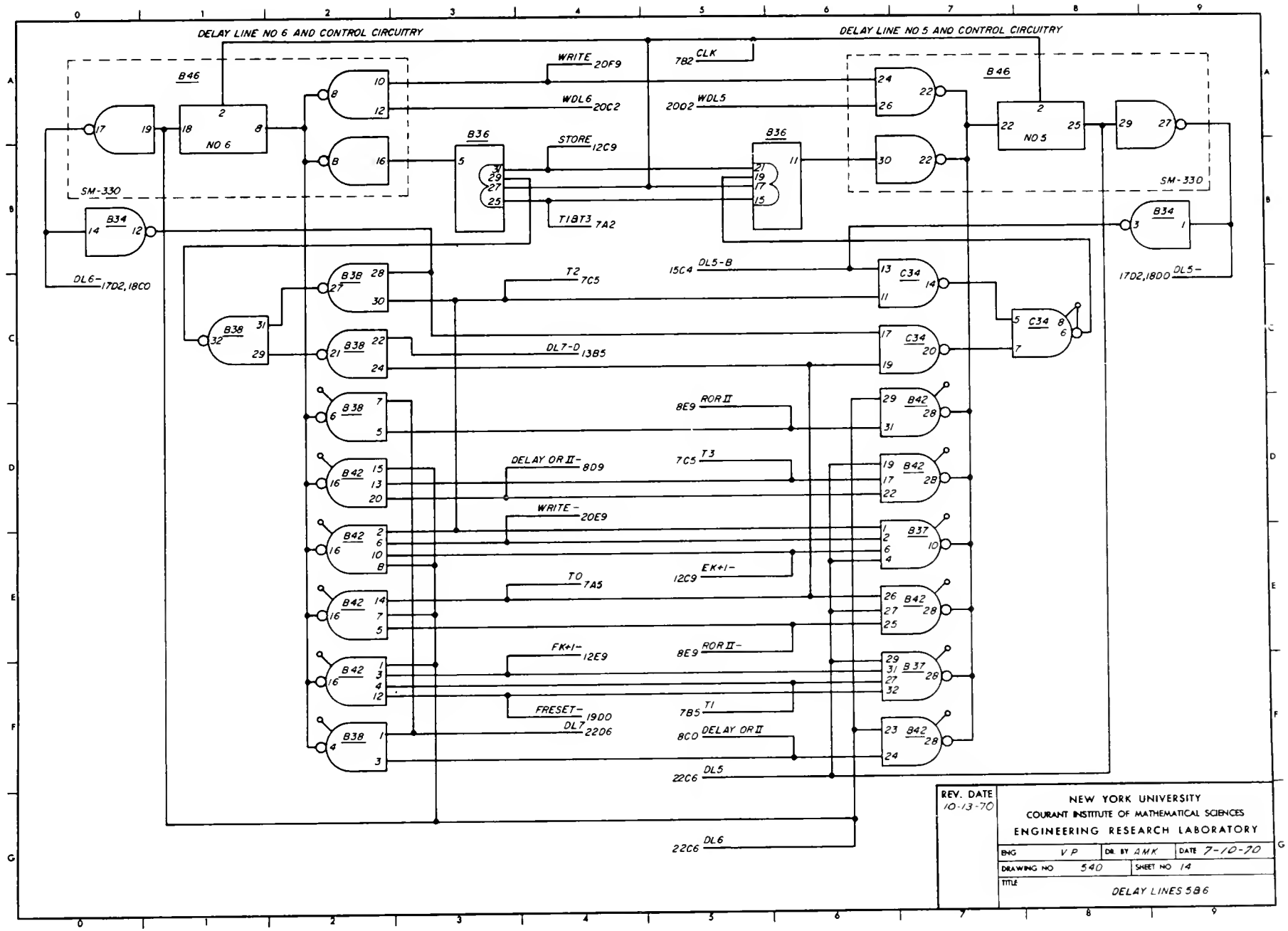
REV. DATE 10-13-70
ENG VP
DR BY A.W.K.
DATE 7-16-70
DRAWING NO 540
SHEET NO 12
TITLE CONTROL LOGIC FOR DELAY LINE 12



REV DATE	NEW YORK UNIVERSITY
10-13-70	COURANT INSTITUTE OF MATHEMATICAL SCIENCES
	ENGINEERING RESEARCH LABORATORY
ENG V.P	DR. BY AMK DATE 7-10-70
DRAWING NO 540	SHEET NO 13
TITLE	DELAY LINES 7&8


DELAY LINE NO 6 AND CONTROL CIRCUITRY
DELAY LINE NO 5 AND CONTROL CIRCUITRY
B46
NO 6
NO 5
SM-330
B34
B36
B37
B38
B42
C34
WRITE 20F9
WDL6 20C2
WDL5 20D2
CLK 7B2
STORE 12C9
T1BT3 7A2
DL6- 17D2, 18C0
DL5- 17D2, 18D0
T2 7C5
DL5-B 15C4
DL7-D 13B5
ROR II 8E9
DELAY OR II- 8D9
T3 7C5
WRITE- 20E9
EK+1- 12C9
T0 7A5
FK+1- 12E9
ROR II- 8E9
FRESET- 19D0
DL7 22D6
T1 7B5
DELAY OR II 8C0
DL5 22C6
DL6 22C6
REV. DATE 10-13-70
NEW YORK UNIVERSITY
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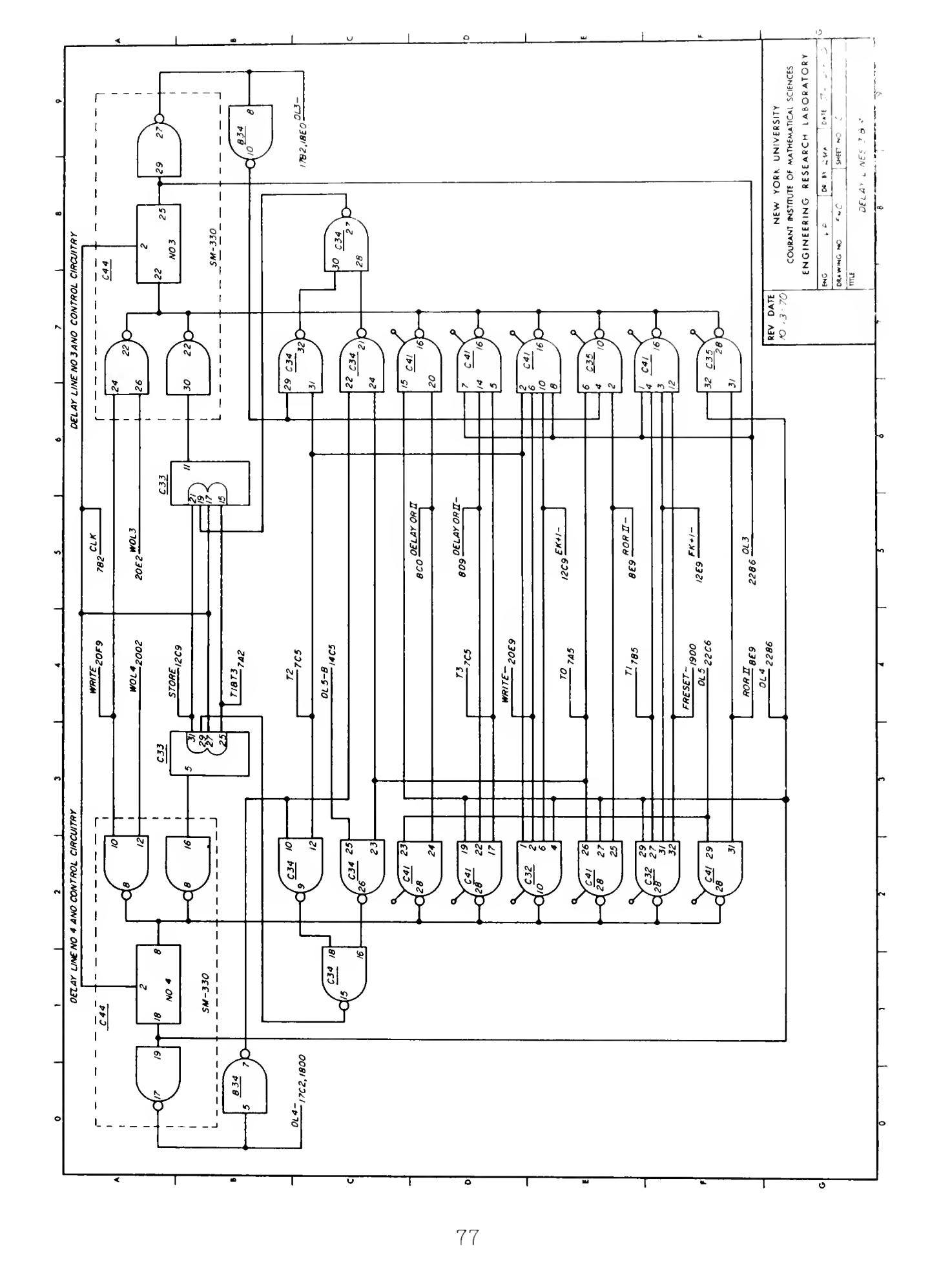
ENGINEERING RESEARCH LABORATORY
ENG V P
DR BY AMK
DATE 7-10-70
DRAWING NO 540
SHEET NO 14
TITLE
DELAY LINES 586


DELAY LINE NO 3 AND CONTROL CIRCUITRY
DELAY LINE NO 4 AND CONTROL CIRCUITRY
SM-330
C44
C33
C34
C41
C32
C35
B34
NO 3
NO 4
782 CLK
20E2 WOL3
WRITE 20F9
WOL4 20D2
STORE 12C9
T1B T3 7A2
T2 7C5
OL5-8 14C5
T3 7C5
WRITE- 20E9
T0 7A5
T1 7B5
FRESET- 19D0
OL5 22C6
ROR II 8E9
OL4 22B6
2286 OL3
8C0 DELAY OR II
8D9 DELAY OR II-
12C9 EK+1-
8E9 ROR II-
12E9 FK+1-
1782,1800 OL4-
1782,18E0 OL3-
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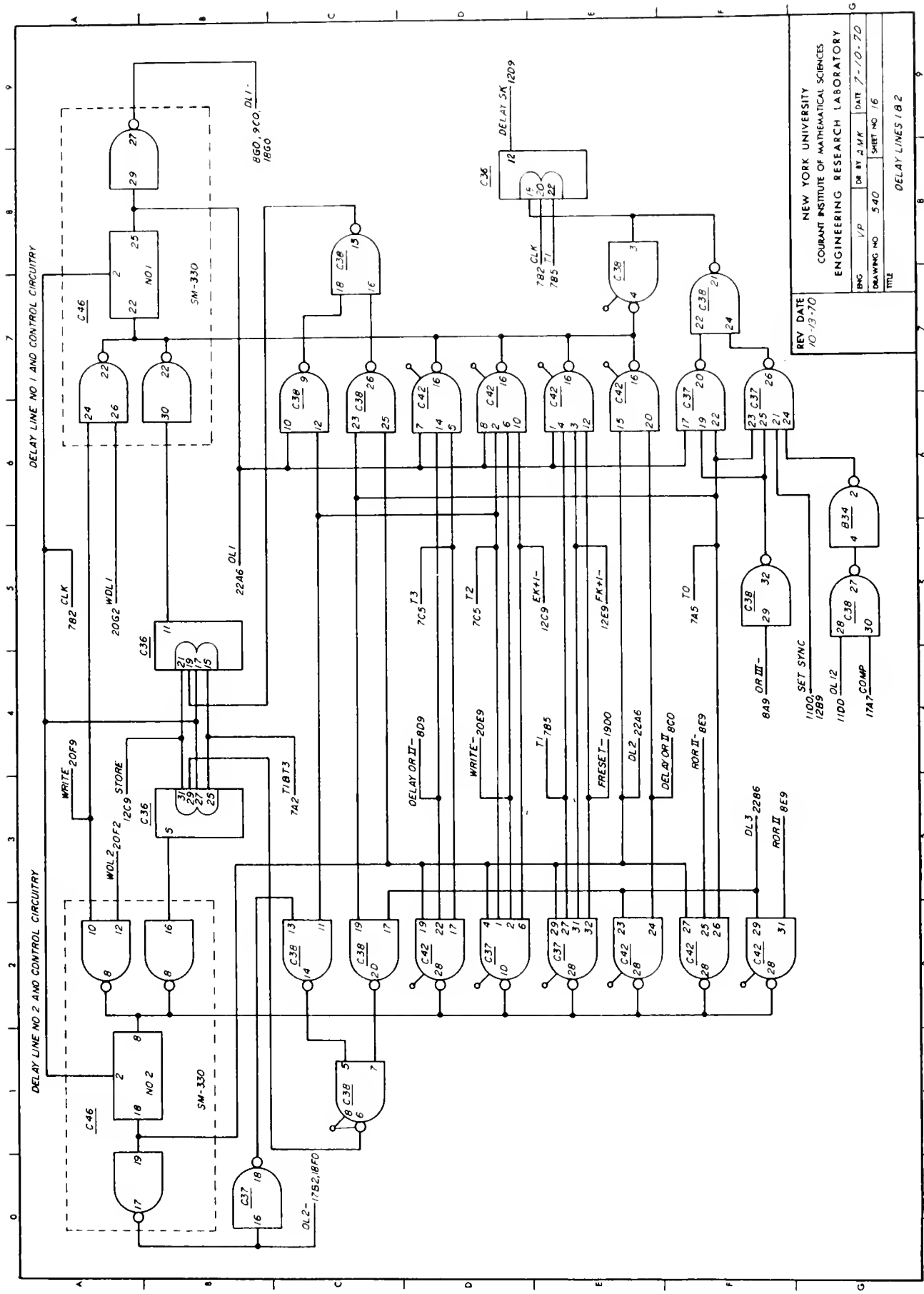
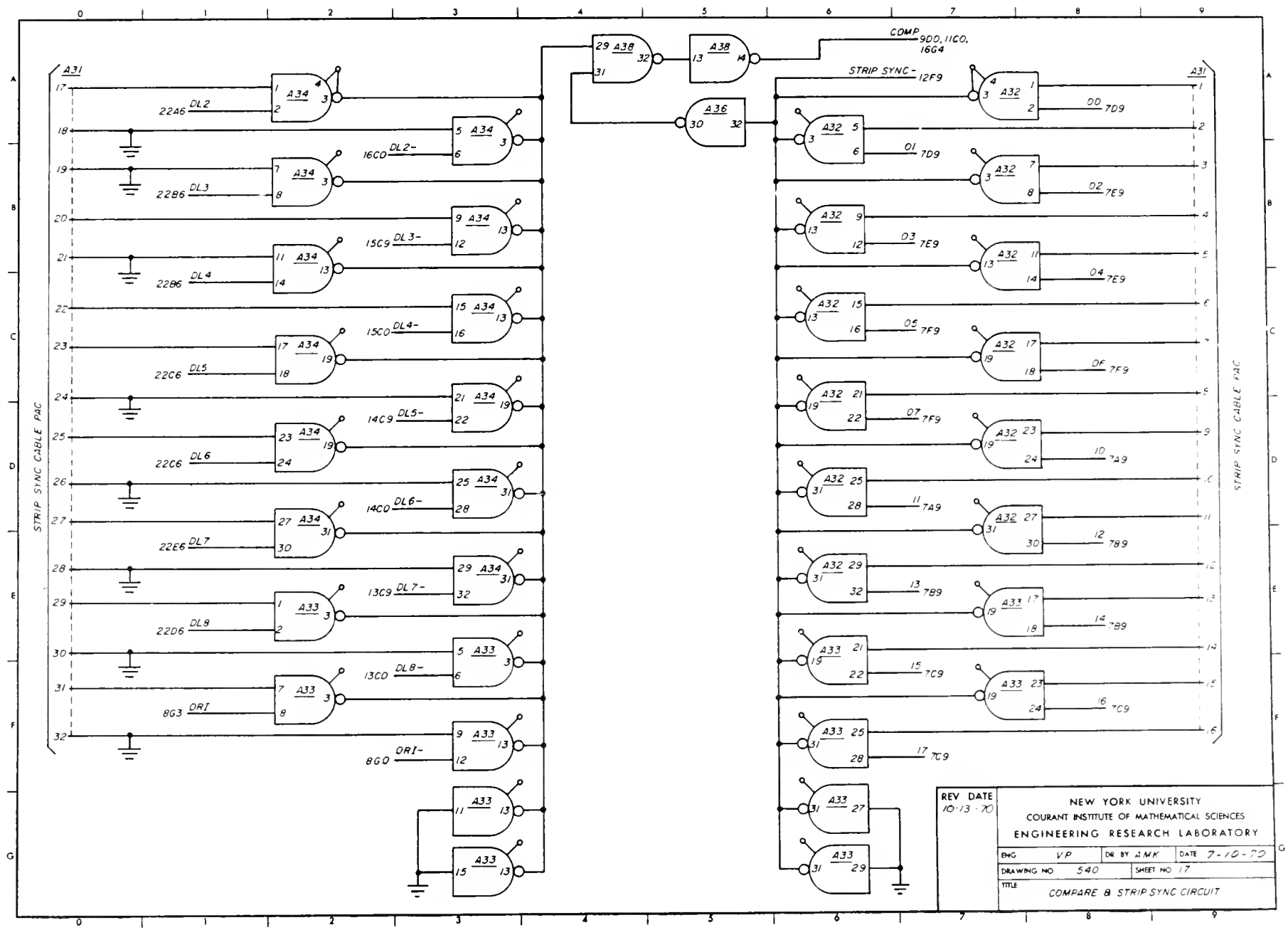
ENGINEERING RESEARCH LABORATORY
REV DATE
10.3.70
ENG
DRAWING NO
TITLE
DELAY LINES


DELAY LINE NO 1 AND CONTROL CIRCUITRY
DELAY LINE NO 2 AND CONTROL CIRCUITRY
SM-330
NO 1
NO 2
C46
C36
C38
C42
C37
782 CLK
20G2 WDL1
WDL2 20F2
WRITE 20F9
12C9 STORE
7A2 T1B13
8GO, 9CO, DL1- 1860
DELAY SK 1209
782 CLK
785 T1
2246 DL1
7C5 T3
7C5 T2
12C9 EK+1-
12E9 FK+1-
DELAY OR II- 809
WRITE- 20E9
T1 785
FRESET- 1900
DL2 2246
DELAY OR II 8C0
ROR II- 8E9
745 T0
DL3 2286
ROR II 8E9
849 OR III-
1100, 1289 SET SYNC
1100 DL12
1174 COMP
834
DL2- 1782, 8F0
REV DATE 10-13-70
NEW YORK UNIVERSITY
COURANT INSTITUTE OF MATHEMATICAL SCIENCES
ENGINEERING RESEARCH LABORATORY
ENG VP
DR BY A.M.K.
DATE 7-10-70
DRAWING NO 540
SHEET NO 16
TITLE DELAY LINES 1 & 2


A31
STRIP SYNC CABLE PAC
22A6 DL2
16C0 DL2-
22B6 DL3
15C9 DL3-
22B6 DL4
15C0 DL4-
22C6 DL5
14C9 DL5-
22C6 DL6
14C0 DL6-
22E6 DL7
13C9 DL7-
22D6 DL8
13C0 DL8-
8G3 ORI
8G0 ORI-
A34
A33
A38
A36
COMP 9DD, 11C0, 16G4
STRIP SYNC - 12F9
A32
00 7D9
01 7D9
02 7E9
03 7E9
04 7E9
05 7F9
0F 7F9
07 7F9
10 7A9
11 7A9
12 7B9
13 7B9
14 7B9
15 7C9
16 7C9
17 7C9
STRIP SYNC CABLE PAC
REV DATE 10-13-70
NEW YORK UNIVERSITY
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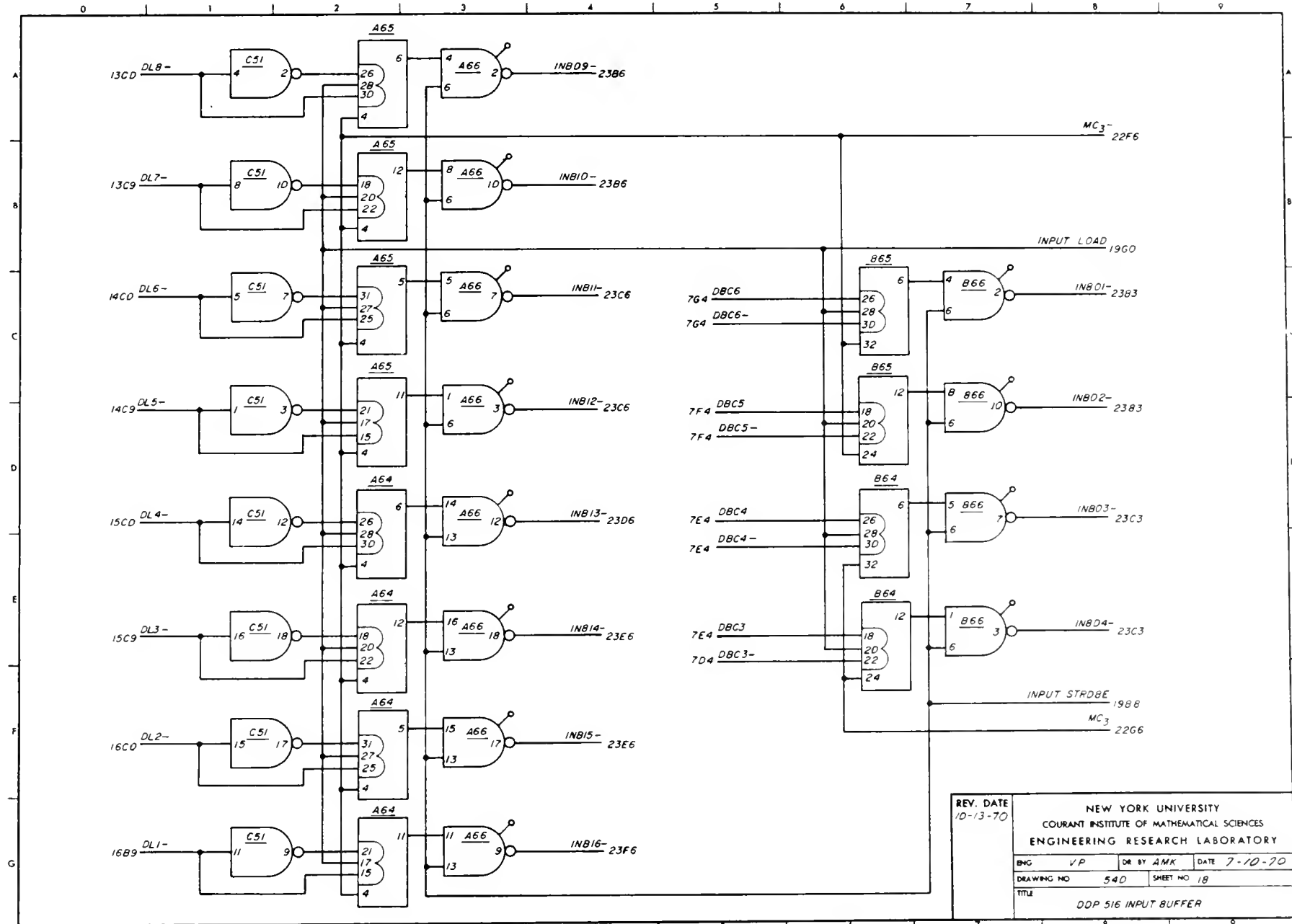
ENGINEERING RESEARCH LABORATORY
ENG VP
DR BY AMK
DATE 7-10-70
DRAWING NO 540
SHEET NO 17
TITLE
COMPARE & STRIP SYNC CIRCUIT


13CD DL8-
13C9 DL7-
14CD DL6-
14C9 DL5-
15CD DL4-
15C9 DL3-
16CD DL2-
16B9 DL1-
C51
A65
A64
A66
INB09- 23B6
INB10- 23B6
INB11- 23C6
INB12- 23C6
INB13- 23D6
INB14- 23E6
INB15- 23E6
INB16- 23F6
MC3- 22F6
INPUT LOAD 19G0
7G4 DBC6
7G4 DBC6-
7F4 DBC5
7F4 DBC5-
7E4 DBC4
7E4 DBC4-
7E4 DBC3
7D4 DBC3-
B65
B64
B66
INB01- 23B3
INB02- 23B3
INB03- 23C3
INB04- 23C3
INPUT STROBE 19B8
MC3 22G6
REV. DATE 10-13-70
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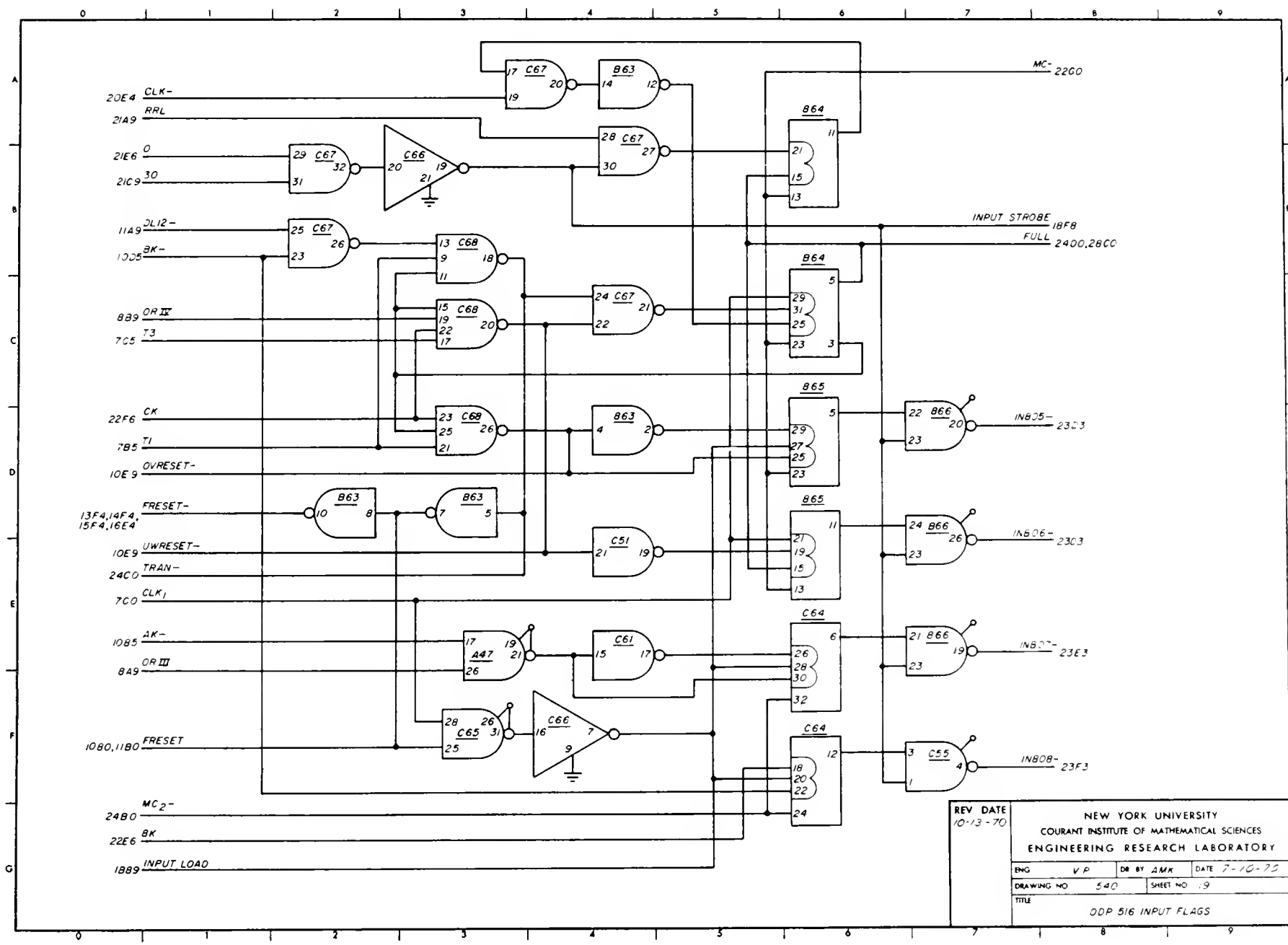
ENGINEERING RESEARCH LABORATORY
ENG VP
DR BY AMK
DATE 7-10-70
DRAWING NO 540
SHEET NO 18
TITLE
DDP 516 INPUT BUFFER


20E4 CLK-
21A9 RRL
21E6 0
21C9 30
11A9 DL12-
1005 BK-
889 OR II
705 T3
22F6 CK
785 TI
10E9 OVRESET-
13F4,14F4, 15F4,16E4 FRESET-
10E9 UWRESET-
24C0 TRAN-
7C0 CLK1
1085 AK-
8A9 OR III
1080,1180 FRESET
24B0 MC2-
22E6 BK
1889 INPUT LOAD
MC- 22G0
INPUT STROBE 18F8
FULL 2400,28C0
INB05- 23D3
INB06- 23D3
INB07- 23E3
INB08- 23F3
C67
C66
C68
B63
B64
B65
B66
C51
C61
A47
C65
C64
C55
REV DATE 10-13-70
NEW YORK UNIVERSITY
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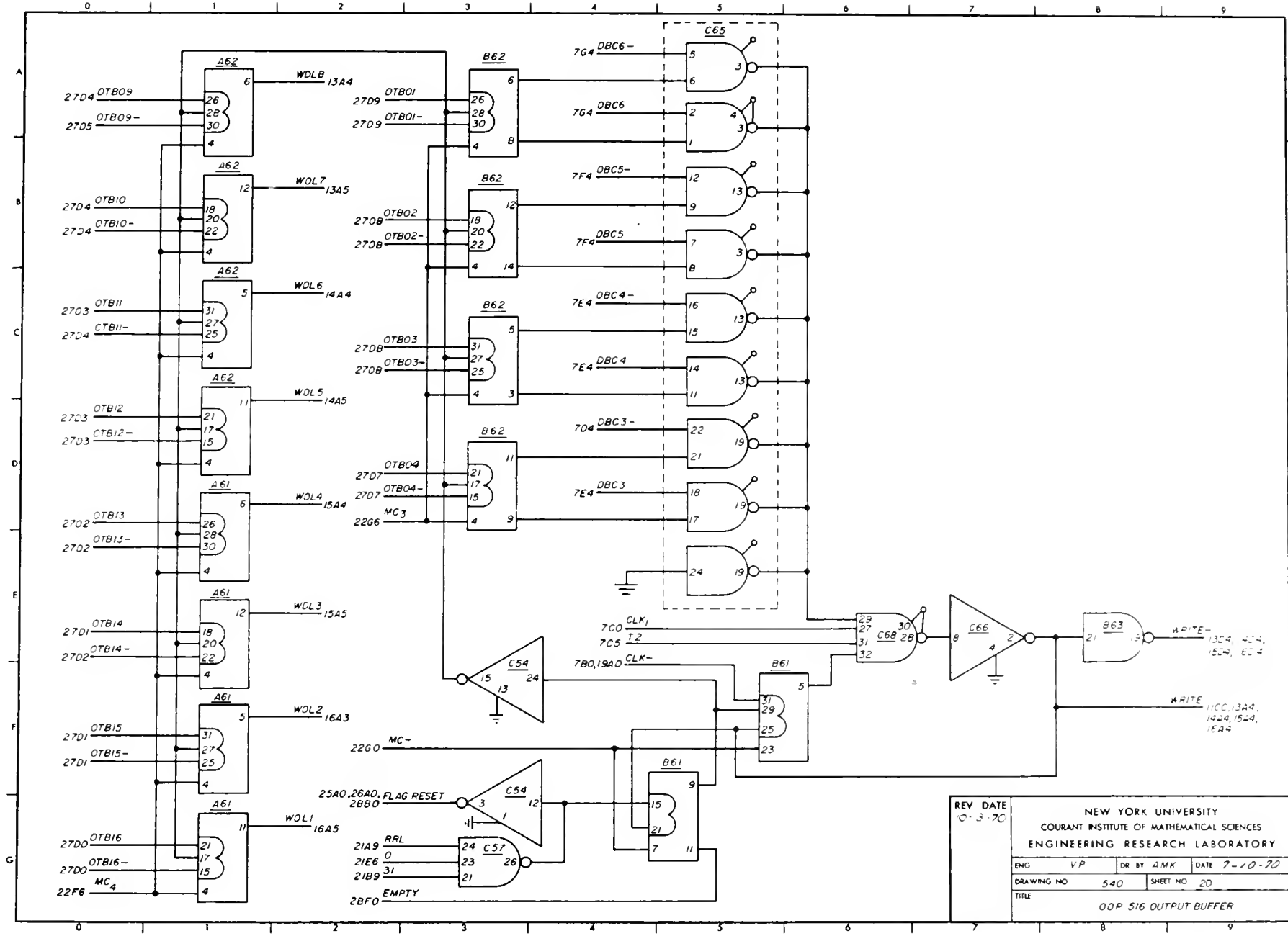
ENG V P
DR BY AMK
DATE 7-10-75
DRAWING NO 540
SHEET NO 19
TITLE
ODP 516 INPUT FLAGS



REV DATE 10-3-70

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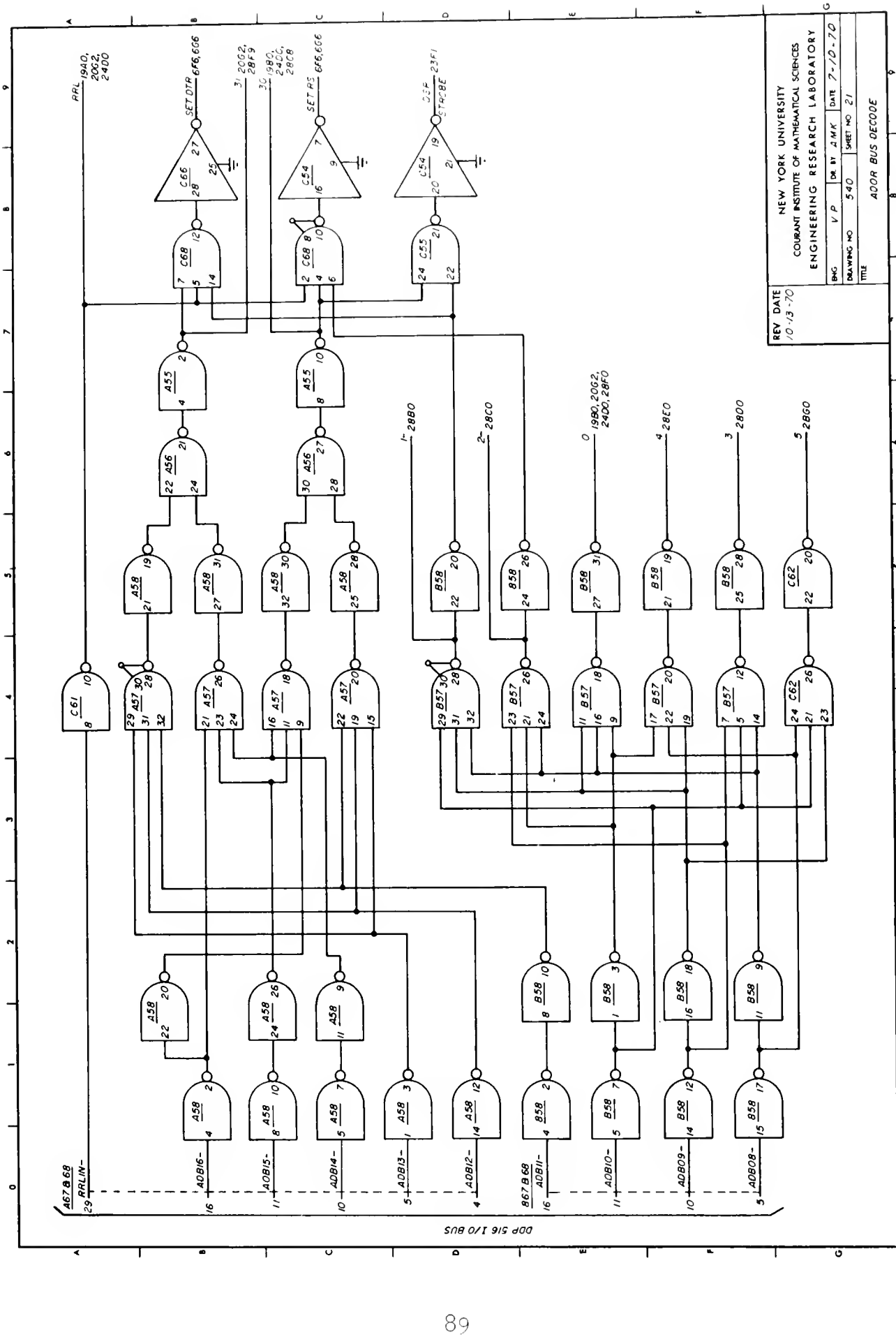
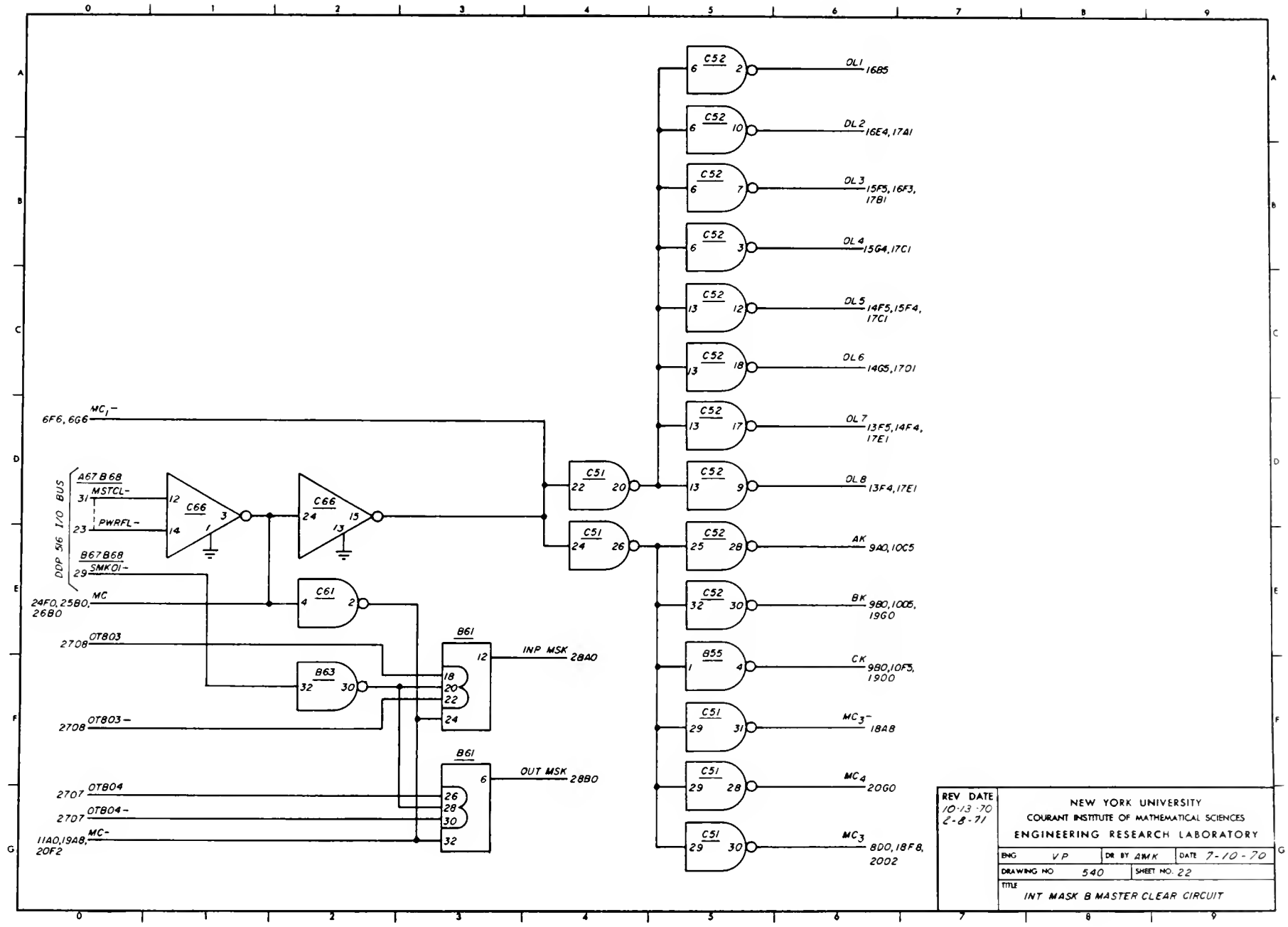
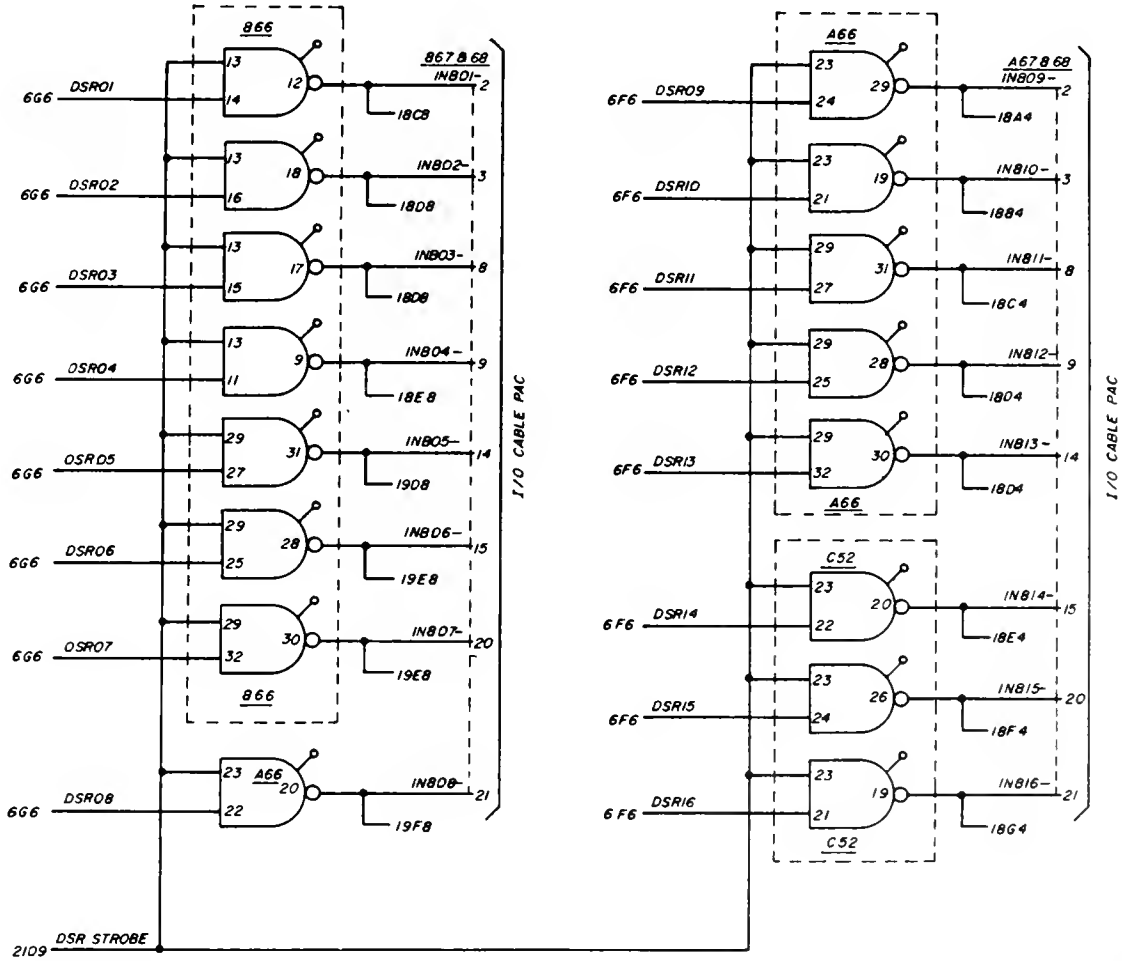
ENG VP	DR BY AMK	DATE 7-10-70
DRAWING NO 540	SHEET NO 20	

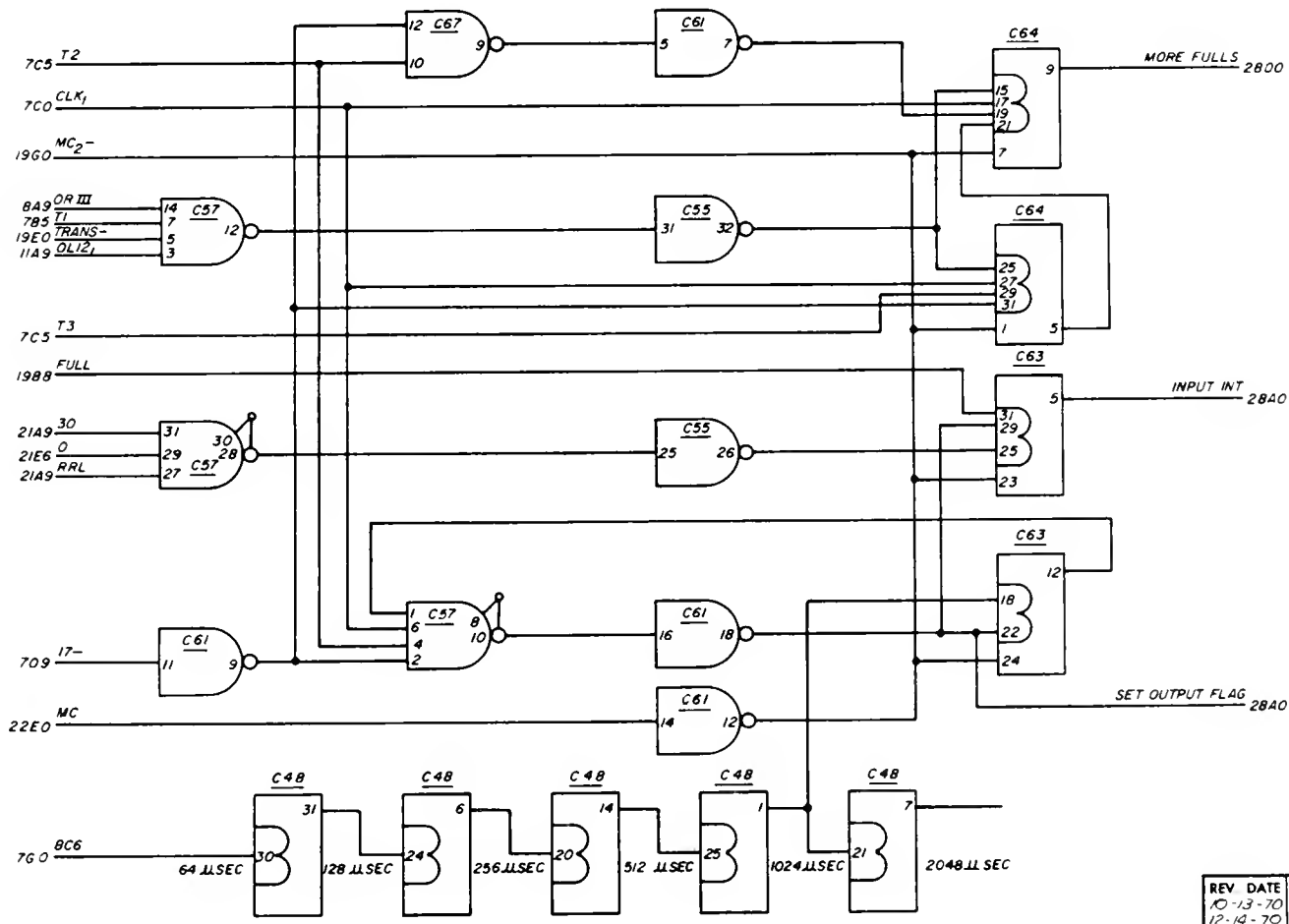
TITLE
OOP 516 OUTPUT BUFFER


NEW YORK UNIVERSITY
COURANT INSTITUTE OF MATHEMATICAL SCIENCES
ENGINEERING RESEARCH LABORATORY
ENG V.P. DR BY AMK DATE 7-10-70
DRAWING NO 540 SHEET NO 21
TITLE ADDR BUS DECODE
REV DATE 10-13-70
DDP 516 I/O BUS
RRL 1940, 2062, 2400
SET DTR 6F6,666
SET RS 6F6,666
CLF STROBE 23F1
1980, 2062, 2400, 28F0
2880
28C0
28E0
2800
28G0
RRLIN-
ADB16-
ADB15-
ADB14-
ADB13-
ADB12-
ADB11-
ADB10-
ADB09-
ADB08-


C52 6 2 OL1 16B5
C52 6 10 OL2 16E4, 17A1
C52 6 7 OL3 15F5, 16F3, 17B1
C52 6 3 OL4 15G4, 17C1
C52 13 12 OL5 14F5, 15F4, 17C1
C52 13 18 OL6 14G5, 17D1
C52 13 17 OL7 13F5, 14F4, 17E1
C52 13 9 OL8 13F4, 17E1
C51 22 20
C51 24 26
C52 25 28 AK 9A0, 10C5
C52 32 30 BK 9B0, 10D5, 19G0
B55 1 4 CK 9B0, 10F3, 19D0
C51 29 31 MC3- 18A8
C51 29 28 MC4 20G0
C51 29 30 MC3 8D0, 18F8, 20D2
6F6, 6G6 MC1-
DDP 516 I/O BUS
A67 B68 MSTCL- 31 12 C66 3 1 14 PWRFL- 23
B67 B68 SMKOI- 29
C66 24 15 13
24F0, 25B0, 26B0 MC
C61 4 2
2708 OT803
B63 32 30
2708 OT803-
B61 12 INP MSK 28A0
18 20 22 24
B61 6 OUT MSK 28B0
26 28 30 32
2707 OT804
2707 OT804-
11A0, 19A8, 20F2 MC-
REV DATE 10-13-70 2-8-71
NEW YORK UNIVERSITY
COURANT INSTITUTE OF MATHEMATICAL SCIENCES
ENGINEERING RESEARCH LABORATORY
ENG VP DR BY AMK DATE 7-10-70
DRAWING NO 540 SHEET NO. 22
TITLE
INT MASK & MASTER CLEAR CIRCUIT



REV DATE 10-13-70	NEW YORK UNIVERSITY COURANT INSTITUTE OF MATHEMATICAL SCIENCES ENGINEERING RESEARCH LABORATORY		
	ENG VP	DR BY AMK	DATE 7-10-70
	DRAWING NO 540	SHEET NO 23	
	TITLE DSR INPUT BUS		



REV	DATE
	10-13-70
	12-14-70

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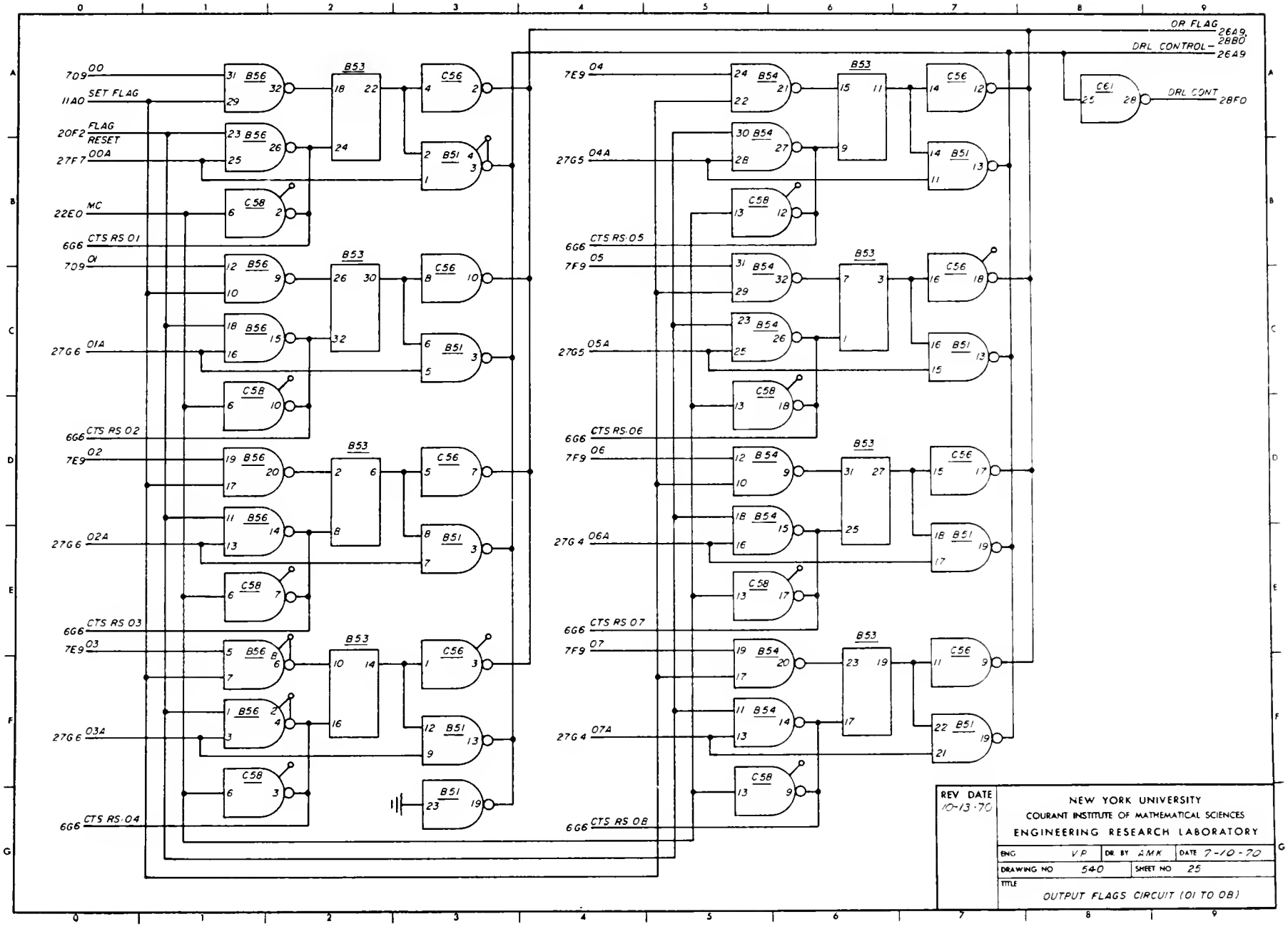
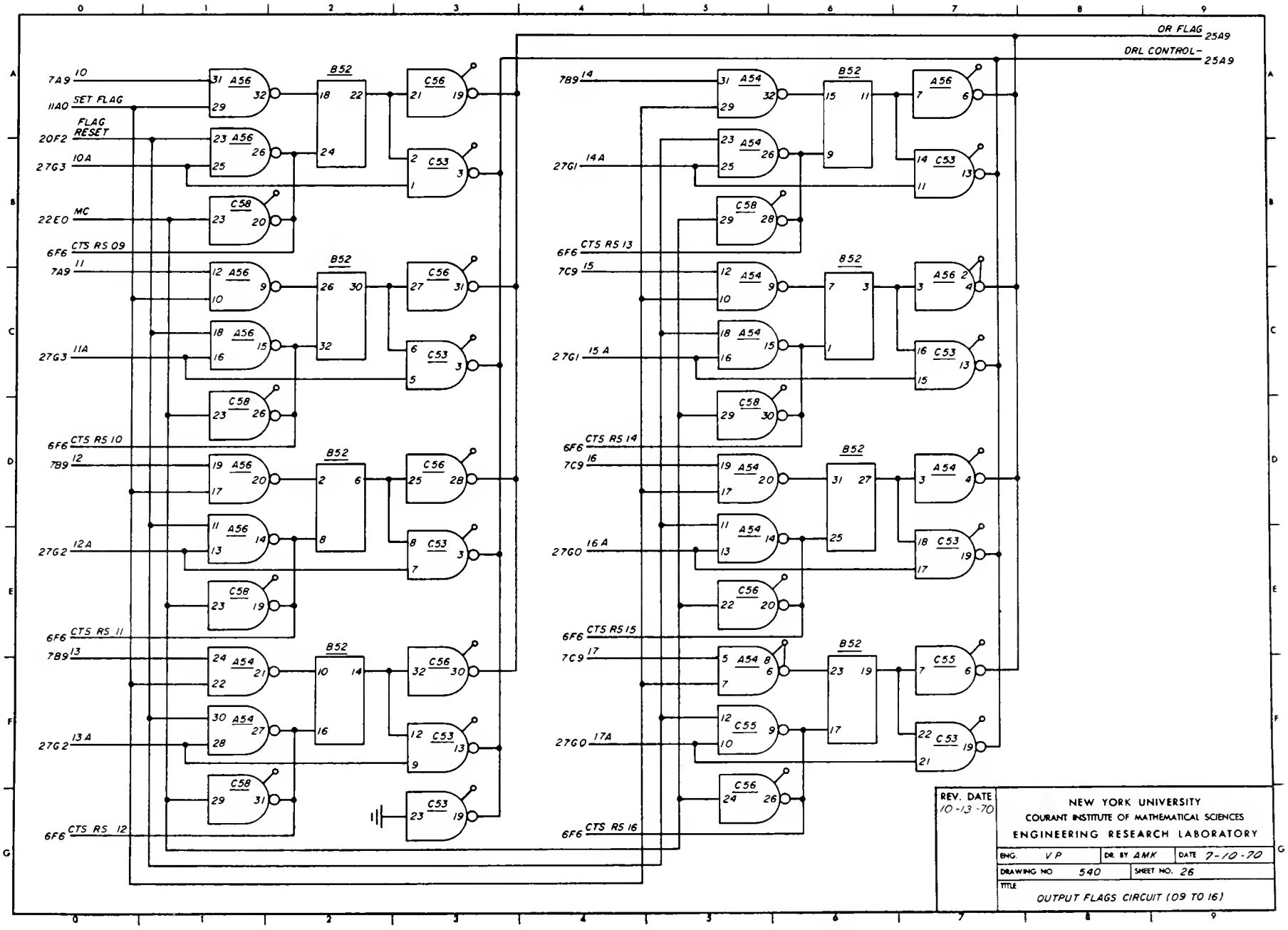
ENG	V P	DR BY AMK	DATE 7-10-70
DRAWING NO	540	SHEET NO. 24	

TITLE: PACER 8 MORE FULLS CIRCUIT


709 00
11A0 SET FLAG
20F2 FLAG RESET
27F7 00A
22E0 MC
6G6 CTS RS 01
709 01
27G6 01A
6G6 CTS RS 02
7E9 02
27G6 02A
6G6 CTS RS 03
7E9 03
27G6 03A
6G6 CTS RS 04
7E9 04
27G5 04A
6G6 CTS RS 05
7F9 05
27G5 05A
6G6 CTS RS 06
7F9 06
27G4 06A
6G6 CTS RS 07
7F9 07
27G4 07A
6G6 CTS RS 08
B56
B53
B51
B54
C56
C58
C61
OR FLAG 26A9, 28B0
DRL CONTROL 26A9
DRL CONT 28F0
REV DATE 10-13-70
NEW YORK UNIVERSITY
COURANT INSTITUTE OF MATHEMATICAL SCIENCES
ENGINEERING RESEARCH LABORATORY
ENG VP
DR BY AMK
DATE 7-10-70
DRAWING NO 540
SHEET NO 25
TITLE
OUTPUT FLAGS CIRCUIT (01 TO 08)


OR FLAG 25A9
DRL CONTROL- 25A9
7A9 10
11A0 SET FLAG
20F2 FLAG RESET
27G3 10A
22E0 MC
6F6 CTS RS 09
7A9 11
27G3 11A
6F6 CTS RS 10
7B9 12
27G2 12A
6F6 CTS RS 11
7B9 13
27G2 13A
6F6 CTS RS 12
7B9 14
27G1 14A
6F6 CTS RS 13
7C9 15
27G1 15 A
6F6 CTS RS 14
7C9 16
27G0 16 A
6F6 CTS RS 15
7C9 17
27G0 17A
6F6 CTS RS 16
A56
A54
B52
C56
C53
C58
C55
REV. DATE 10-13-70
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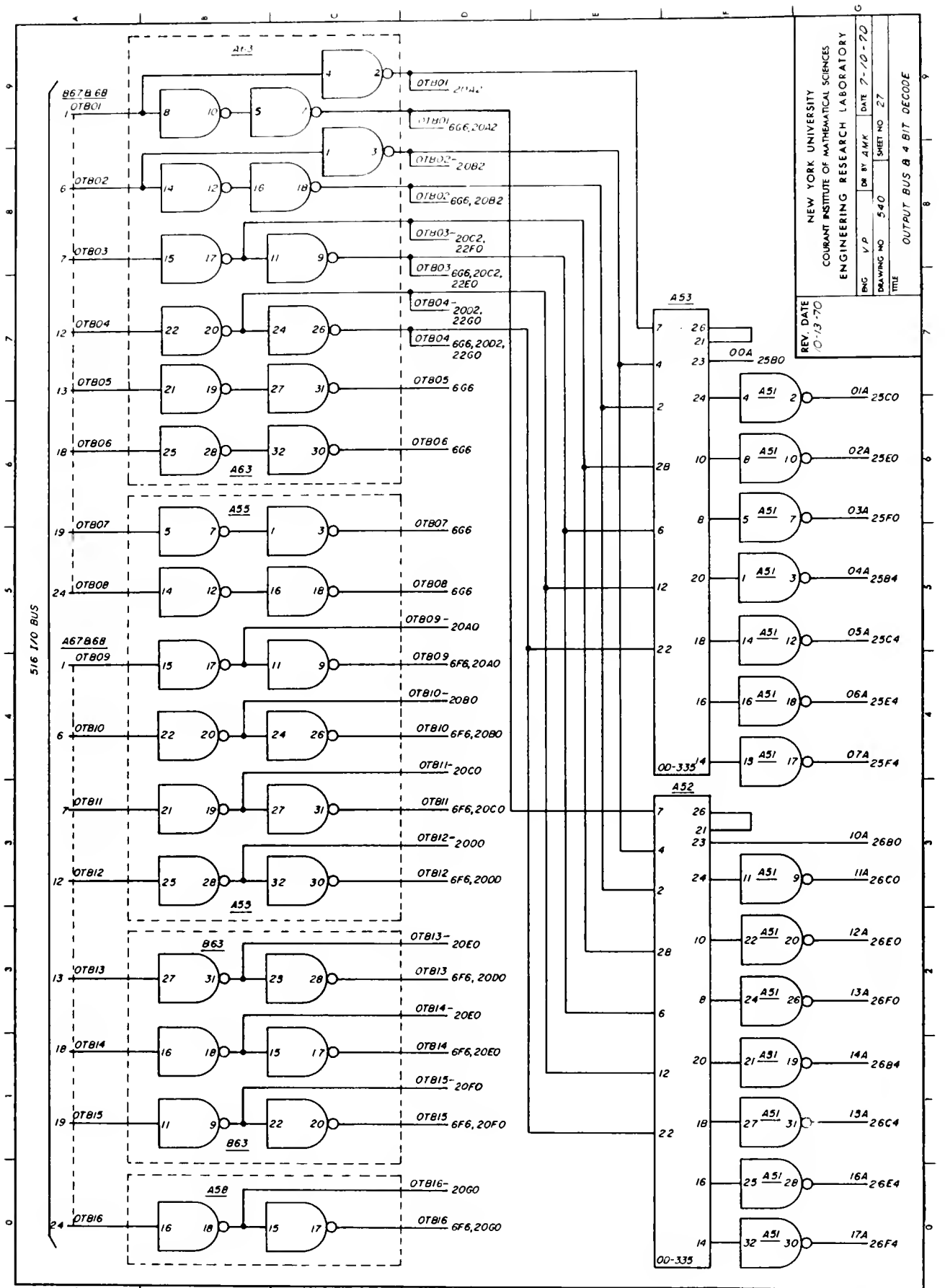
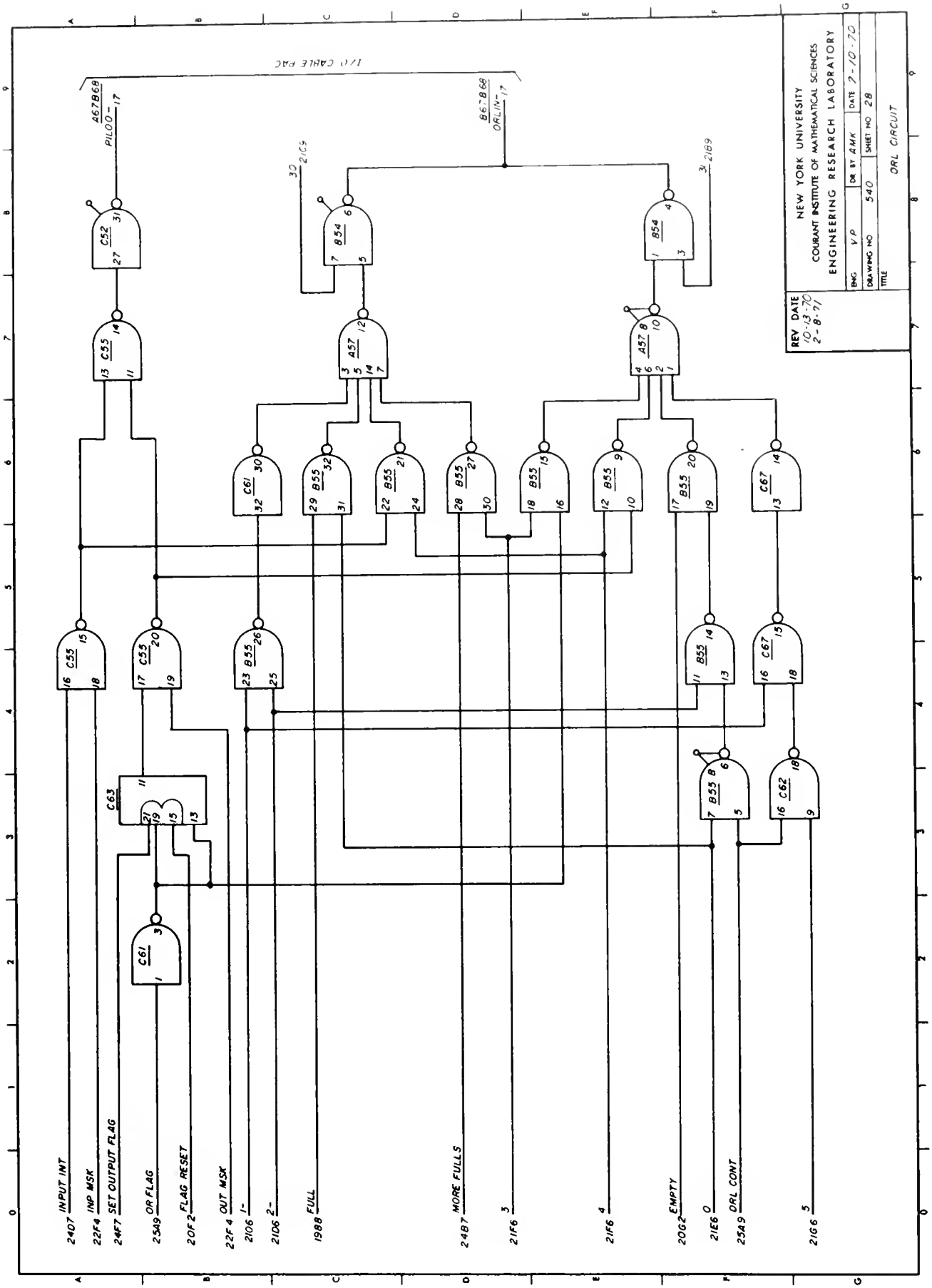
ENGINEERING RESEARCH LABORATORY
ENG. V P
DR. BY AMK
DATE 7-10-70
DRAWING NO. 540
SHEET NO. 26
TITLE
OUTPUT FLAGS CIRCUIT (09 TO 16)


NEW YORK UNIVERSITY
COURANT INSTITUTE OF MATHEMATICAL SCIENCES
ENGINEERING RESEARCH LABORATORY
DR BY AMK
DATE 7-10-70
SHEET NO 27
DRAWING NO 540
ENG
VP
TITLE
OUTPUT BUS B 4 BIT DECODE
REV. DATE 10-13-70
516 I/O BUS
B67 B 68
OTB01
OTB02
OTB03
OTB04
OTB05
OTB06
OTB07
OTB08
OTB09
OTB10
OTB11
OTB12
OTB13
OTB14
OTB15
OTB16
A63
A55
B63
A58
A53
A52
A51
00A
01A
02A
03A
04A
05A
06A
07A
10A
11A
12A
13A
14A
15A
16A
17A
00-335
25B0
25C0
25E0
25F0
25B4
25C4
25E4
25F4
26B0
26C0
26E0
26F0
26B4
26C4
26E4
26F4


I/O CABLE PAC
467868 PILOO- 17
867868 ORLIN- 17
NEW YORK UNIVERSITY
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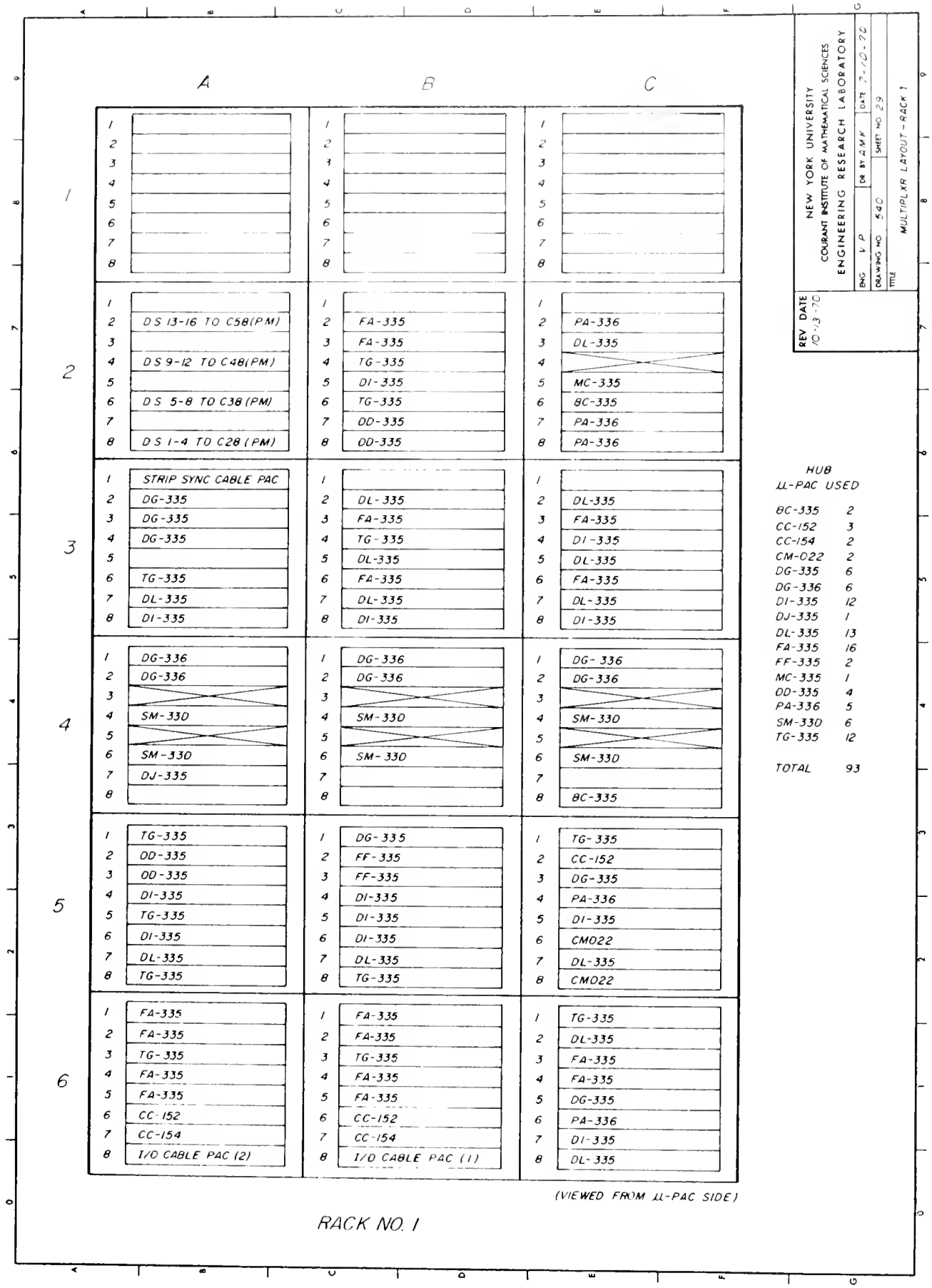
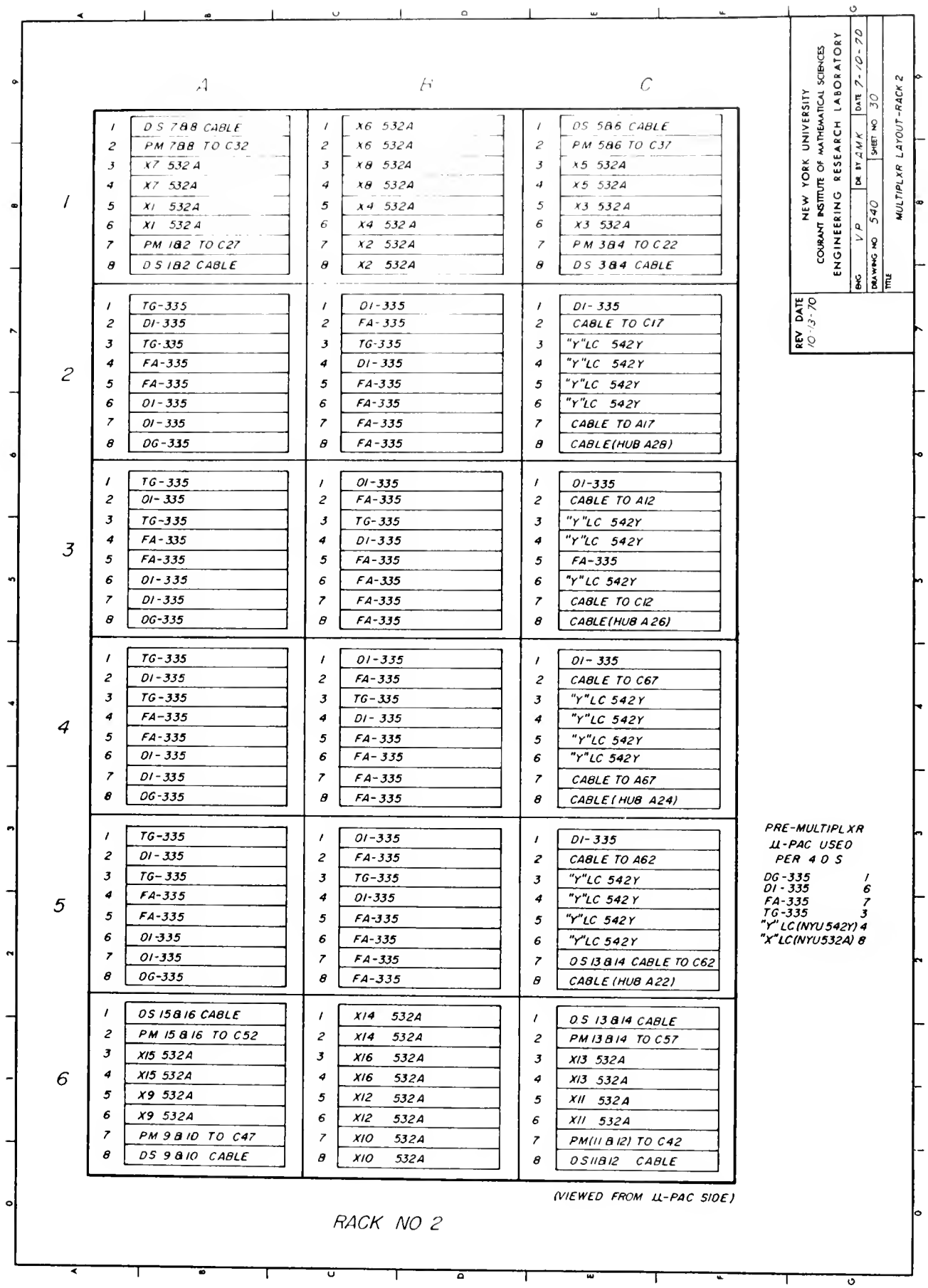
ENGINEERING RESEARCH LABORATORY
REV DATE 10-13-70 2-8-71
ENG VP
DR BY AMK
DATE 2-10-70
DRAWING NO 540
SHEET NO 28
TITLE ORL CIRCUIT
2407 INPUT INT
22F4 INP MSK
24F7 SET OUTPUT FLAG
2349 OR FLAG
20F2 FLAG RESET
22F4 OUT MSK
2106 1-
2106 2-
1988 FULL
2487 MORE FULLS
21F6 3
21F6 4
2062 EMPTY
21E6 0
2349 ORL CONT
2166 5



HUB
LL-PAC USED

BC-335	2
CC-152	3
CC-154	2
CM-022	2
DG-335	6
DG-336	6
DI-335	12
DJ-335	1
DL-335	13
FA-335	16
FF-335	2
MC-335	1
DD-335	4
PA-336	5
SM-330	6
TG-335	12
TOTAL	93


NEW YORK UNIVERSITY
COURANT INSTITUTE OF MATHEMATICAL SCIENCES
ENGINEERING RESEARCH LABORATORY
ENG VP
DR BY AMK
DATE 7-10-70
DRAWING NO 540
SHEET NO 30
TITLE MULTIPLXR LAYOUT-RACK 2
REV DATE 10-3-70
A
B
C
1
DS 788 CABLE
PM 788 TO C32
X7 532A
X7 532A
X1 532A
X1 532A
PM 182 TO C27
DS 182 CABLE
X6 532A
X6 532A
X8 532A
X8 532A
X4 532A
X4 532A
X2 532A
X2 532A
DS 586 CABLE
PM 586 TO C37
X5 532A
X5 532A
X3 532A
X3 532A
PM 384 TO C22
DS 384 CABLE
2
TG-335
DI-335
TG-335
FA-335
FA-335
DI-335
DI-335
DG-335
DI-335
FA-335
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DI-335
CABLE TO A17
"Y"LC 542Y
"Y"LC 542Y
"Y"LC 542Y
"Y"LC 542Y
CABLE TO A17
CABLE(HUB A28)
3
TG-335
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DG-335
DI-335
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FA-335
FA-335
FA-335
FA-335
DI-335
CABLE TO A12
"Y"LC 542Y
"Y"LC 542Y
FA-335
"Y"LC 542Y
CABLE TO C12
CABLE(HUB A26)
4
TG-335
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DI-335
DI-335
DG-335
DI-335
FA-335
TG-335
DI-335
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FA-335
FA-335
DI-335
CABLE TO C67
"Y"LC 542Y
"Y"LC 542Y
"Y"LC 542Y
"Y"LC 542Y
CABLE TO A67
CABLE(HUB A24)
5
TG-335
DI-335
TG-335
FA-335
FA-335
DI-335
DI-335
DG-335
DI-335
FA-335
TG-335
DI-335
FA-335
FA-335
FA-335
FA-335
DI-335
CABLE TO A62
"Y"LC 542Y
"Y"LC 542Y
"Y"LC 542Y
"Y"LC 542Y
DS 13814 CABLE TO C62
CABLE (HUB A22)
6
DS 15816 CABLE
PM 15816 TO C52
X15 532A
X15 532A
X9 532A
X9 532A
PM 9810 TO C47
DS 9810 CABLE
X14 532A
X14 532A
X16 532A
X16 532A
X12 532A
X12 532A
X10 532A
X10 532A
DS 13814 CABLE
PM 13814 TO C57
X13 532A
X13 532A
X11 532A
X11 532A
PM(11812) TO C42
DS11812 CABLE
PRE-MULTIPLXR
μ-PAC USED
PER 405
DG-335 1
DI-335 6
FA-335 7
TG-335 3
"Y" LC(NYU542Y) 4
"X"LC(NYU532A) 8
(VIEWED FROM μ-PAC SIDE)
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